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Modeling and Harmonic Performance of a 12- AC-DC Power Converter with Diode-Clamped Multilevel Inverter for Induction Motor Drives

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Abstract

This study presents the modelling and harmonic performance analysis of a 12-pulse AC-DC power converter integrated with a five-level diode-clamped multilevel inverter (DCMLI) for high-power induction motor drive applications. It includes system architecture, simulation results, and comparative evaluation against conventional designs. Traditional six-pulse rectifier-based variable frequency drives (VFDs) typically generate significant low-order harmonics—specifically the 5th, 7th, 11th, and 13th, which contribute to poor power factor, voltage distortion, and increased energy consumption. To address these limitations, a 12-pulse DC-AC power converter was developed using phase-shifted transformers to suppress dominant harmonics. Additionally, the DCMLI employs advanced pulse-width modulation (PWM) strategies—namely Phase Disposition (PD), Phase Opposition Disposition (POD), and Alternate Phase Opposition Disposition (APOD) to enhance inverter output quality. Simulation results obtained via MATLAB/Simulink demonstrate that the 12-pulse DC-AC power converter reduces input current total harmonic distortion (THD) from 69.84% (in the six-pulse configuration) to 62.23%, while improving the input power factor from 0.43 to 0.58. Output voltage THD for the DCMLI using APOD PWM is 17.97%, compared to 18.09% and 18.40% for PD and POD techniques, respectively. The proposed system configuration yields smoother motor torque, a 24.73% reduction in rectifier output voltage ripple, and approximately 25% improvement in energy efficiency over the conventional six-pulse drive. Overall, the integration of a 12-pulse rectifier significantly enhances harmonic performance, power factor, and energy efficiency in DCMLI-based induction motor drive systems.

Keywords: *Diode-Clamped, Harmonic, Distortion, Induction Motor, Variable Frequency Drive, V/F Control.*

1. INTRODUCTION

Induction motors represent a category of fixed-speed motors predominantly used across various industrial sectors due to their cost-effectiveness, efficiency, and robust design. In any industrial applications that need variable speed operation, the application of induction motors is constrained due to its constant speed. A variable frequency drive constitutes a specific type of adjustable speed drive, which is alternatively designated as AC drives. This device regulates the operational speed of the electric machine by transforming the grid frequency into modifiable values at the machine side, thereby facilitating the electric motor's rapid and efficient adaptation to the desired speed [1]. Variable frequency drives are employed across different industrial drives like milling machines, compressors, blowers and pump [1]. Many

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industrial applications that require variable speed uses Variable Frequency Drives (VFD) to control their induction motor; this can be attributed to their capability to not only facilitate variable speed control for induction motors but also to enhance constant torque at different speed variation. Substantial energy conservation is achieved during the operation of the motor at reduced speeds. Furthermore, VFDs contribute to the enhancement of both dynamic and steady-state performance characteristics of the motor [2],[4],[5]. The diode rectifier utilizes passive component to mitigate harmonic issues, but this approach creates a more complex system, especially in applications that uses 415V and above. The 6-pulse rectifier is commonly used in most AC drives due to its affordability and straightforward design [6], without a harmonics filter, the input current Total Harmonic Distortion (THD) can exceed 100%, displaying dominant 5th, 7th, and 11th harmonics under full load conditions. The harmonics filter primarily addresses the 5th, 7th, and 11th harmonics, which are the most prominent harmonic components [3],[6]. The key benefit of this research is that the modeling is done to enhance the total harmonics distortion, power factor improvement and energy optimization which will improve induction motor performance especial in an industrial where dynamic loading of the motor is paramount.

2. LITERATURE REVIEW

Variable frequency drives are employed across different industrial drives like milling machines, compressors, blowers and pump [1]. The authors in [1] worked on the modeling, simulation, and performance analysis of a variable frequency drive (VFD) for speed control of an induction motor using MATLAB/Simulink. They developed a VFD system model and analyzed its effectiveness in controlling the speed of an induction motor under various load conditions. They realized that the VFD provided efficient and precise speed control, improved energy savings, and better dynamic response compared to conventional methods. But their work focuses mainly on the basic VFD configuration without addressing advanced issues such as harmonic distortion, multi-pulse rectification, or integration of multilevel inverter topologies. This study in [2] discussed the advantages of VFDs, such as energy savings and improved dynamic performance, while outlining key industrial applications. However, the review did not capture detailed modeling or simulation result, how to mitigate some harmonics introduced by Variable frequency drives (VFDs) and integration of multilevel inverter technologies. This result in [3] compares open-loop and closed-loop speed control techniques using sinusoidal PWM. The study concludes that closed-loop SPWM is superior, offering real-time adaptability and reduced Total Harmonic Distortion (THD). Despite its contributions, the study simplifies load conditions and lacks exploration of advanced industrial PWM methods like level shifted PWM, and the use of 12 pulses instead of 6 pulses which could improve harmonic performance and power quality. The methodology of this study in [4] covers only open-loop control strategy which is not mostly used in speed variation in industrial application, also it does not integrate12-pulse rectifier and multilevel inverters which can provide lesser harmonics to the speed drive. While the study demonstrates the benefits of PWM, additionally, the paper focuses on steady-state performance under constant and variable loads but does not examine dynamic response conditions of the induction motor, which are crucial for practical motor control systems.

2.1 Twelve (12)-Pulse Transformer and Rectifier

The design of 12-pulse transformers involves creating a particular phase shift to allow the transformer to operate with 12-pulse converter systems [7],[8]. . The study in [7],[8]

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highlighted that 12-pulse rectifiers are effective in eliminating 5th and 7th harmonics, which helps to improved power factor and reduced Total Harmonic Distortion (THD) in the input current, The study in [7-8], highlighted the importance of 12-pulse transformer in aerospace and effect of inbuilt filter in12-pulse transformer but the design is not use to drive induction motor with the diode clamped multilevel inverters. Power quality reduction-especially harmonic distortion and power factor, are a major concern in rectifier-based systems [9], [10]. The author in [10] proposed an advanced method to reduce harmonic distortion by connecting a filter network at the output of the diode bridge rectifier. Their study also demonstrated that this method reduces the harmonics present, improved the THD and improves the power factor of the power system network which the rectifier is connected. The authors presented an analytical model in Simulink, followed by simulation and experimental validation, proving the effectiveness of the filter network in power conversion systems. The findings suggested that this passive filtering approach provides a cost-effective alternative to active harmonic filters, which are more costly, making it economically suitable for industrial applications where power quality improvements are very important. Similarly, the study conducted in [9] indicates that the incorporation of DC chokes in rectifiers further dampens current ripples, resulting in a more consistent DC output. This form of rectification can be either controlled or uncontrolled. These studies [9], [10] highlighted the importance of 12-pulse rectifier but the effects of multilevel inverters are not captured.

2.2 Multilevel Inverters

In order to enhance the power quality, efficiency and harmonic performance in induction motor drives [11]–[15], many multilevel inverter (MLI) and multi-pulse converter systems have been developed. The developed performance of the three-level diode clamped and T-type inverter topologies are presented [11]. The THD and Switching losses was less for varying modulations. The DG-link capacitors employed in MLIs have also been analyzed to reliability in hard industrial environment for stable operation. Therefore, improvements in design-for-reliability (DfR) are necessary [12]. To improve the quality of power and lower input current harmonics through the technique of transformer phase displacement, the study in [13] has implemented a hybrid multilevel multi-pulse converter. The cascaded H-bridge multilevel inverter has also proved to have better THD, lower switching losses and better torque in EV motor drive [14]. To enhance multilevel inverters' switching performance, various modulation techniques have been developed. One method, sinusoidal pulse width modulation (SPWM), uses different triangular carrier signals to produce switching pulses. It is easy to implement [16]. It is good for low to medium voltage applications. However, it has relatively high switching losses when the voltage is high as pointed in [16]. The more sophisticated strategy known as space vector modulation (SVM) optimizes the switching patterns for inverter states that are represented spatially; this method applies specially to a high-power drive and an industrial application because it reduces total harmonic distortion (THD) and switching losses [17]. Another commonly used method is the selective harmonic elimination (SHE), where switching angles are modified to eliminate the 5th, 7th, 11th and 13th harmonics, therefore leaving out the need for extra filters [18]. Even though the method reduces harmonics effectively, it involves solving nonlinear equations, which adds to its complexity. Multilevel inverters are widely used in renewable energy sources, multilevel inverters in HVDC transmission reduces the harmonic pollution associated with long-distance power transmission, and it can also be found in electric vehicles and rail traction systems, where they support the efficient conversion of electric power for traction motors [19][20] [21]. According to [19][20] [21] multilevel will summarized in Table 1

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Table 1 Comprehensive Comparison of Multilevel Inverter (MLI) Topologies

Feature	Diode-Clamped MLI (DCMLI)	Capacitor-Clamped MLI (CCMLI)	Cascaded H-Bridge MLI (CHBMLI)
Voltage Levels	Fixed with clamping diodes	Floating capacitors for level balancing	Modular design with series-connected H-bridges
Complexity	High due to multiple diodes	High due to capacitor balancing	Moderate; requires multiple DC sources
Harmonic Reduction	Good (depends on levels)	Excellent (better balancing)	Best (modular and scalable)
Control Complexity	Moderate	High (capacitor balancing required)	Lower compared to others
Efficiency	High	High but capacitor losses exist	Highest (lower switching losses)
Modularity	Low (difficult to expand)	Low (complex capacitor arrangement)	High (easy to scale with more H-bridges)
Diode Clamping	Essential for voltage balancing	Not used	Not required
Capacitor Equalization	Not required	Critical for voltage stability	Not required
Applications	Industrial motor drives, HVDC	High-voltage applications	Renewable energy, electric vehicles, power grid integration

3. SYSTEM MODELING AND METHODOLOGY

The proposed system includes a 12-pulse rectifier, a DC link filter, a five-level diode-clamped offline multilevel inverter (DCMLI), and an induction motor drive module. The system was modeled and simulated using MATLAB/Simulink. The 12-pulse transformer has one primary winding and two secondary windings. Its secondary windings have star-star and star-delta connections. This results in a 30° phase shift between the outputs. The input current waveform is optimized through the use of phase shift cancelling 5th 7th Harmonics the complete system block diagram is shown in Figure1

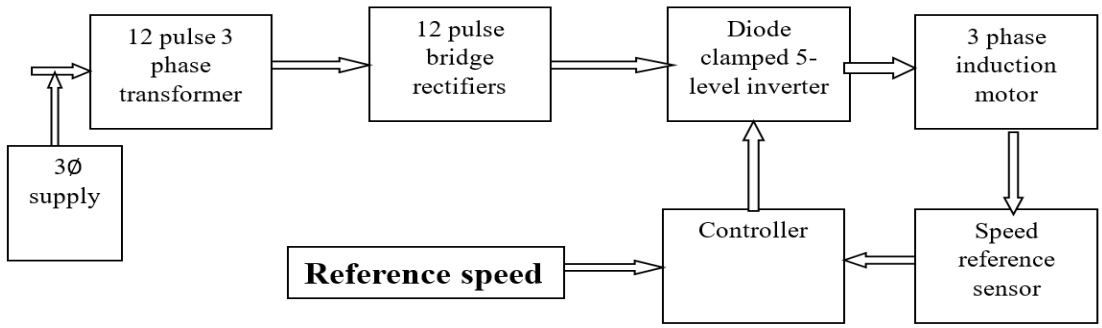

Figure 1 block diagram of the complete system

3.1 12-Pulse Transformer and Twelve-Pulse Full-Bridge Rectifier Model

With 6KW (8Hp,$50Nm$) shaft power but for reliable design 10% of the load is added to the selected transformer for optimal and dynamic performance. Also the secondary side voltage of a transformer used in VFD for industrial purposes are always bigger than RMS value of the induction motor to be connected to it, this is to account for voltage drop in power electronics

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devices during switching the transformer model is shown in Figure 1. The E.m.f equation for primary and secondary winding are represented equations **(1)** and (2) .

$$V_P = 4.44f\ N_P\varphi_m \tag{1}$$

$$V_S = 4.44f\ N_S\varphi_m \tag{2}$$

The rectifier in Figure 2 is designed base on the output power of 7.5kW, using the equation **(3)** the output voltage $V_{dc}$of the rectifier can be calculated as shown in equation **(6)**

Average voltage V_{dc} of any rectifier if given

$$V_{dc} = \frac{1}{2\pi}\int_0^{2\pi} V_m \sin \omega t\, d\omega t \tag{3}$$

$$V_{dc} = -\frac{3V_m}{\pi}\{-1\}$$

$$V_{dc} = \frac{3V_m}{\pi} \tag{4}$$

Also to calculate the V_m (maximum voltage) equation is used as

$$V_m = \sqrt{2}V_{L-L} \tag{5}$$

Therefore the V_{dc} will be calculate in times of line to line r.m.s voltage as shown in equation (6)

$$V_{dc} = \frac{3\sqrt{2}}{\pi}V_{L-L} \tag{6}$$

$$V_{dc} = \frac{3\sqrt{2}}{\pi} * 470\ = 634.72\text{V} \tag{7}$$

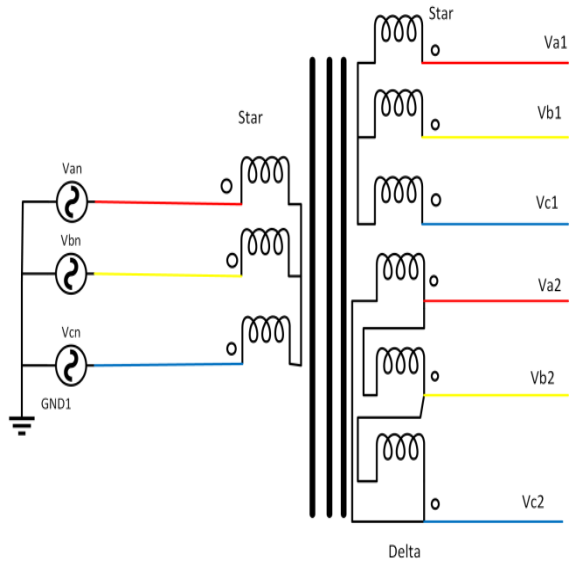

Figure 1 model of 12 pulse transformer

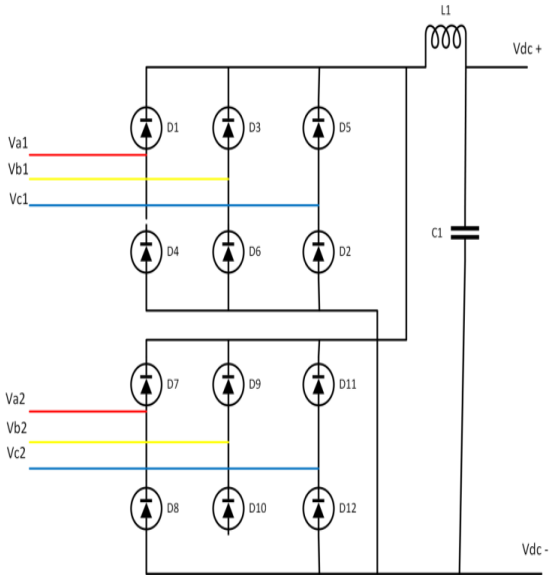

Figure 2 model of 12- pulse rectifier

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According to Figure 3 and Figure 4 line to line voltage of secondary star transformer is lead 30 degrees to line to neutral voltage. Line to line voltage of secondary delta transformer is in phase with line to neutral voltage. Therefore, total output voltage waves of two transformers are shifted 30 degree each other. The output voltage magnitudes of two transformers must same. Due to the parallel connection, output current flowing through the two converters divided between them.

Therefore, rating of the transformer is 10KVA, 415V/470V pf 0.85; 50Hz 12 pulse dry type transformer and diodes ratings are Peak inverse voltage of 1300V and average forward current of 7A,

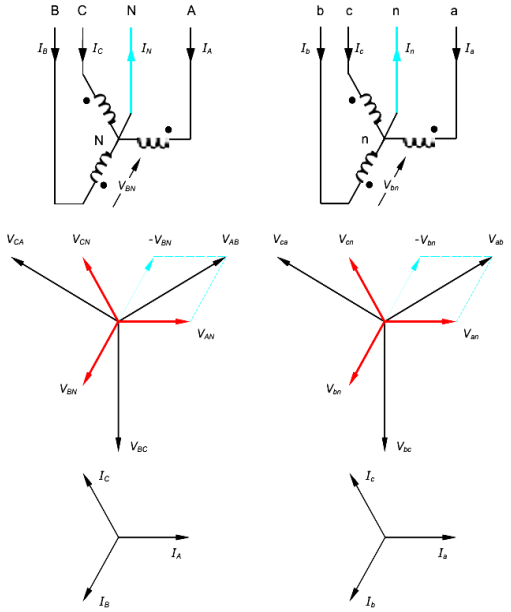

Figure 3 Winding arrangement and Phasor Diagrams of Y-Y transformer

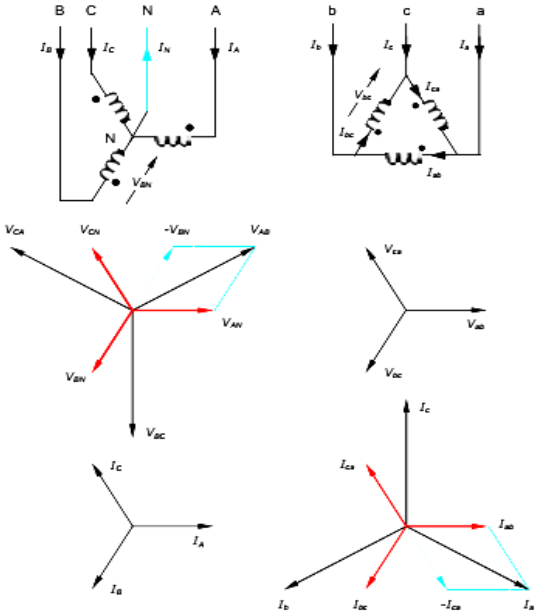

Figure 4 Winding arrangement and Phasor Diagrams of Y-Δ transformer

In this study the 12-pulse rectifier is gotten by parallel connection of two six (6) pulse rectifier, therefore the maximum voltage of the 12 pulses output which is the algebraic summation of the six pulses is the same as the maximum voltage of six pulses but contains interleaved pulses that leads to the twelve pulse. The switching table of the diodes is shown in Table 1 and Table 2 which shows the diodes conducting in every full-cycle and also how the currents flow

Table 1 Upper six (6) diode bridge rectifier the switching table

S/N	SECTOR	D1	D2	D3	D4	D5	D6	Line voltage across l	Current path
1	$330 \leq \omega t \leq 30°$	1	1	0	0	0	0	Vac1 (va1- vc1)	Va1→D1→load→ D2→ vc1
2	$30° \leq \omega \leq 90°$	0	1	1	0	0	0	Vbc1(vb1- vc1)	vb1→D2→load→ D3→ vc1
3	$90° \leq \omega \leq 150°$	0	0	1	1	0	0	Vab1 (va1- vb1)	vb1→D3→load→ D4→ va1
4	$150° \leq \omega t \leq 210°$	0	0	0	1	1	0	Vac1(va1- vc1)	Va1→D4→load→ D5→ vc1
5	$210° \leq \omega t \leq 270°$	0	0	0	0	1	1	Vbc1(vb1- vc1)	vb1→D5→load→ D6→ vc1
6	$270° \leq \omega t \leq 330°$	1	0	0	0	0	1	Vab1(va1- vb1)	vb1→D3→load→ D4→ va1

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Table 2 Lower Six (6) Diode Bridge Rectifier the Switching Table

S/N	SECTOR	D7	D8	D9	D10	D11	D12	Line voltage across l	Current path
1	$360 \leq \omega t \leq 60°$	0	0	1	0	0	1	Vbc2(vb2- vc2)	Vb2→D9→load→ D12→ vc2
2	$60° \leq \omega \leq 120°$	0	1	1	0	0	0	Vab2(va2- vb2)	Vb2→D9→load→ D8→ Va2
3	$120° \leq \omega \leq 180°$	0	1	0	0	1	0	Vac2(va2- vc2)	Vc2→D11→load→ D8→ Va2
4	$180° \leq \omega t \leq 240°$	0	0	0	1	1	0	Vbc2(vb2- vc2)	Vc2→D11→load→ D10→ Vb2
5	$240° \leq \omega t \leq 300°$	1	0	0	1	0	0	Vab2(va2- vb2)	Va2→D7→load→ D10→ vb2
6	$300° \leq \omega t \leq 360°$	1	0	0	0	0	1	Vac2 (va1- vc1)	Va2→D7→load→ D12→ Vc2

3.2. Diode-Clamped Multilevel Inverter (DCMLI) Design

A five-level DCMLI is implemented to improve the inverter's output waveform, reducing THD and enhancing efficiency and the quality of the waveform, which will help to increase the motor performance and the lifespan. The DCMLI is feed by the filtered 12-pulse rectifier output, through the help of the modulation strategies it produces a staircase AC voltage waveform that are approximately a sinusoidal waveform and perform better than traditional inverter. The MATLAB/Simulink model of 5 levels DCMLI is shown in Figure 5.

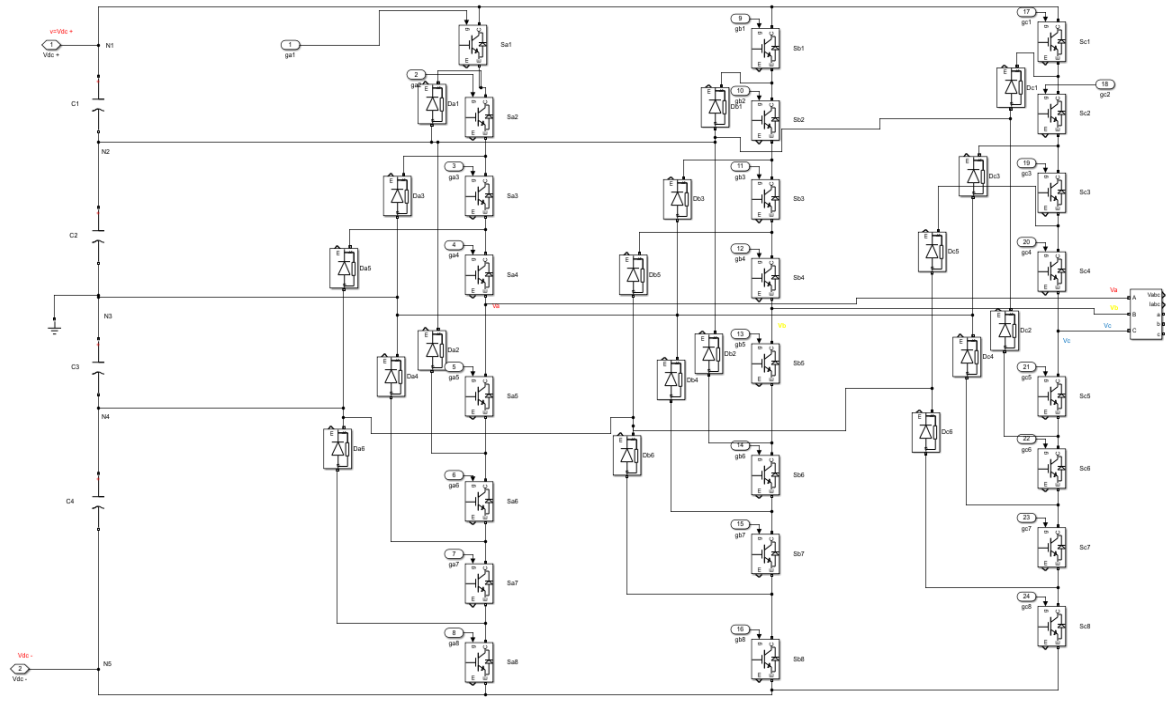

Figure 5 MATLAB/Simulink model of 5 levels DCMLI

The total DC bus voltage is divide into four (4) by the capacitors forming five (5) nodes as shown in equation (12) , therefore each capacitor voltage is given by equation (

$$V_c = \frac{V_{dc}}{4} \tag{8}$$

The five node potential is with respect to neutral can be generated. For integer selector p_x for phase x ∈ {a, b, c), $p_x \in \{-2, -1, 0, 1, 2\}$

From the integer p_x the phase voltage of the phase x with respect the neutral point N is give by

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$$V_{xN} = p_x \frac{V_{dc}}{4} \quad (8)$$

For phase a voltage is given in equation ((9) is developed by using $p_a \in \{-2, -1, 0, 1, 2\}$ using equation (8), the levels of V_{aN} is given by equation (9)

$$V_{aN}, V_{bN} \in \{+\frac{V_{dc}}{2}, \quad +\frac{V_{dc}}{4}, \quad 0, = -\frac{V_{dc}}{4}, \quad -\frac{V_{dc}}{2}, \} \quad (9)$$

To get the line-to-line voltages V_{ab} is given by

$$V_{ab} = (V_{aN} - V_{bN}) = (p_a - p_b)\frac{V_{dc}}{4} \quad (10)$$

Where $(p_a - p_b) \in \{-4, -3, -2, -1, 0, 1, 2, 3, 4\}$ for conduction period the level of line to line voltage is given by

$$V_{ab} \in \{-V_{dc}, -\frac{3V_{dc}}{2}, -\frac{V_{dc}}{2}, -\frac{V_{dc}}{4}, 0, = \frac{V_{dc}}{4}, \frac{V_{dc}}{2}, \frac{3V_{dc}}{2}, V_{dc}, \} \quad (11)$$

In a balanced PWM operation with coordinated switching across the phase the $\frac{3V_{dc}}{2}, -\frac{V_{dc}}{4}$ component happens at a very instant of time therefore the component is not available in the line-to-line voltages, and the final levels is given by equation (**12**)

$$V_{ab} \in \{-V_{dc}, \quad -\frac{V_{dc}}{2}, \quad 0, \quad \frac{V_{dc}}{2}, \quad V_{dc}, \} \quad (12)$$

Each phase leg of the 5-level DCMLI selects one of five discrete phase voltages relative to the DC midpoint by switching groups of MOSFETs as stated in equation (9) and, where necessary, using clamping diodes to connect to intermediate capacitor junctions. Table 3 and Table 4 show the list of the switch groups and the likely diode paths for Phase A and Phase B at each phase level referenced to the neutral.

Table 3 five (5)-level DCMLI performance and current flow during switching for phase A

p_a	Phase Voltage (V_{aN})	Phase A switches ON	Clamping diode status for A	Conduction path
+2	$\frac{V_{dc}}{2}$	Sa1,Sa2,Sa3,Sa4	None	$+\frac{V_{dc}}{2}(N1) \rightarrow$ Sa1→Sa2 → Sa3 → Sa4→ Va→Load→Neutral(N3)
+1	$\frac{V_{dc}}{4}$	Sa2,Sa3,Sa4,Sa5	Da1 and Da2 will possible conduct	$+\frac{V_{dc}}{4}(N2) \rightarrow$ Da1→Sa2 → Sa3 → Sa4→ Va→Load→Neutral(N3), the returning path can be through Sa5, Da2 to the C2 to Neutral(N3)
0	0	Sa3,Sa4,Sa5,Sa6	Da3 and Da4 will possible conduct	Neutral(N3) →Da3→Sa3 → Sa4 →Va→Load→Neutral(N3), the returning path can be through Sa5, Sa6, Da4 to Neutral(N3)
-1	$-\frac{V_{dc}}{4}$	Sa4,Sa5,Sa6 Sa7	Da5 and Da6 will possible conduct	$-\frac{V_{dc}}{4}(N4) \rightarrow$ Da6→Sa7 → Sa6 → Sa5→ Va→Load→Neutral(N3), the returning path can be through Sa4, Da5 to the C3 to Neutral(N3)
-2	$-\frac{V_{dc}}{2}$	Sa5,Sa6,Sa7,Sa8	None	$-\frac{V_{dc}}{2}(N5) \rightarrow$ Sa8→Sa7 → Sa6 → Sa5→ Va→Load→ Neutral(N3)

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Table 4 five (5)-level DCMLI performance and current flow during switching for phase B

p_b	Phase Voltage (V_{aN})	Phase B switches ON	Clamping diode status for B	Conduction path
+2	$\frac{V_{dc}}{2}$	Sb1,Sb2,Sb3,Sb4	None	$+\frac{V_{dc}}{2}(N1) \rightarrow$ Sb1→Sb2 → Sb3 → Sb4→ Vb→Load→Neutral(N3)
+1	$\frac{V_{dc}}{4}$	Sb2,Sb3,Sb4,Sb5	Db1 and Db2 will possible conduct	$+\frac{V_{dc}}{4}(N2) \rightarrow$ Db1→Sb2 → Sb3 → Sb4→Vb→Load→Neutral(N3), the returning path can be through Sb5, Db2 to the C2 to Neutral(N3)
0	0	Sb3,Sb4,Sb5,Sb6	Db3 and Db4 will possible conduct	Neutral(N3) →Db3→Sb3 → Sb4 →Vb→Load→Neutral(N3), the returning path can be through Sb5, Sb6, Db4 to Neutral(N3)
-1	$-\frac{V_{dc}}{4}$	Sb4,Sb5,Sb6 Sb7	Db5 and Db6 will possible conduct	$-\frac{V_{dc}}{4}(N4) \rightarrow$ Db6→Sb7 → Sb6 → Sb5→Vb→Load→Neutral(N3), the returning path can be through Sb4, Db5 to the C3 to Neutral(N3)
-2	$-\frac{V_{dc}}{2}$	Sb5,Sb6,Sb7,Sb8	None	$-\frac{V_{dc}}{2}(N5) \rightarrow$ Sb8→Sb7 → Sb6 → Sb5→ Vb→Load→ Neutral(N3)

Table 5 shows how particular (Va,Vb) pairings produce the five principal line-to-line voltages as stated in equation (12), the corresponding switch groups, diode status and the A→B current path. Intermediate instantaneous voltages (e.g. ±Vdc/4 or ±3Vdc/4) can occur briefly during switching transitions but do not form the sustained bins in coordinated PWM operation.

Table 5 five (5)-level DCMLI performance and current flow during switching for line-line (VAB)

Line Voltage level	Example (V_{aN}, V_{bN}), (p_a, p_b)	Phase A switches ON	Phase B switches ON	Clamping diode status for (A/B)	Conduction path
V_{dc}	$(+\frac{V_{dc}}{2}, -\frac{V_{dc}}{2})$, (+2,-2)	Sa1, Sa2, Sa3,Sa4	Sb5, Sb6, Sb7,Sb8	None/None	$+V_{dc}$ → Sa1→Sa2 → Sa3 → Sa4→ Va→Load→Vb→Sb5→Sb6→ Sb7→Sb8→ $-V_{dc}$
$\frac{V_{dc}}{2}$	$(+\frac{V_{dc}}{2}, 0)$,(+2, 0)	Sa1, Sa2, Sa3,Sa4	Sb3, Sb4, Sb5,Sb6	None/ (Db3 Db4 will possible conduct)	$\frac{V_{dc}}{2}(N1)$ →Sa1→Sa2 →Sa3 →Sa4→Va→Load→ Vb→Sb4→Sb3→Db3→ Neutral(N3), Or $\frac{V_{dc}}{2}(N1)$ →Sa1→Sa2→Sa3→Sa4→Va→Load→ Vb→Sb5→Sb6→Db4→ Neutral(N3),
0	(0 , 0),(0, 0)	Sa3, Sa4, Sa5,Sa6	Sb3, Sb4, Sb5,Sb6	Da3 Da4 Db3 Db4 will possible conduct	Neutral(N3) →Da3→Sa3 →Sa4 →Va→Load→ Vb→Sb4 →Sb3→Db3→ Neutral(N3), Or Neutral(N3) →Da3→Sa3 →Sa4 →Va→Load→ Vb→Sb5 →Sb6→Db4→ Neutral(N3),
$-\frac{V_{dc}}{2}$	$(0, +\frac{V_{dc}}{2})$, (0, +2)	Sa3, Sa4, Sa5,Sa6	Sb1, Sb2, Sb3,Sb4	(Db3 Db4 will possible conduct)/ None	Neutral(N3)→Da4→Sa6→Sa5→Va→Load→ Vb→Sb4→Sb3→Sb1→ $\frac{V_{dc}}{2}(N1)$ Or Neutral(N3)→Da3→Sa3→Sa4→Va→Load→ Vb→Sb4→Sb3→Sb1→ $\frac{V_{dc}}{2}(N1)$
$-V_{dc}$	$(-\frac{V_{dc}}{2}, +\frac{V_{dc}}{2})$, (-2,+2)	Sa5, Sa6, Sa7,Sa8	Sb1, Sb2, Sb3,Sb4	None/None	$-V_{dc}$ →Sa8→Sa7→Sa6→Sa5→Va→Load→ Vb→Sb4→Sb3→Sb2→Sb1→ $+V_{dc}$

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3.3 Modulation Strategy

To generate gate signals for the IGBTs used for the 5-level diode clamped multilevel inverter (DCML), multicarrier sinusoidal pulse width modulation (PWM) techniques is used. The modulation strategies implemented where phase disposition (PD), phase opposition disposition (POD), and alternate phase opposition disposition (APOD), the reason for using three different PWM techniques was to determine the one that has less THD and also its effect on the induction motor dynamics.

Each of these PWM has 4 different carrier signal with the same frequency and one reference signal for each phase, the carrier signals are the same for the three phases just that the modulating signal (reference signal) are 120° phase shifted making the gate signal shifted also to generate three phase balance voltage from the inverter output.

3.4 Modeling of Induction Motor

The stator voltage equations are given in equation (13)

$$V_{as} = i_{as}r_s + \frac{d\lambda_{as}}{dt}$$
$$V_{bs} = i_{bs}r_s + \frac{d\lambda_{bs}}{dt} \quad (13)$$
$$V_{cs} = i_{cs}r_s + \frac{d\lambda_{cs}}{dt}$$

The rotor voltage equations are shown below in equation(14)

$$V_{ar} = i_{ar}r_r + \frac{d\lambda_{ar}}{dt}$$
$$V_{br} = i_{br}r_r + \frac{d\lambda_{ar}}{dt} \quad (14)$$
$$V_{cr} = i_{cr}r_r + \frac{d\lambda_{cr}}{dt}$$

Since machine and power system parameters are nearly always given in ohms or percent or per unit of base impedance, it is convenient to express the voltage and flux linkage equations in terms of reactance rather than inductance and the equivalent circuit is shown below in equation (15)

$$v_{qs} = r_s i_{qs} + \frac{\omega}{\omega_b}\varphi_{ds} + \frac{\rho}{\omega_b}\varphi_{qs}$$
$$v_{ds} = r_s i_{qs} - \frac{\omega}{\omega_b}\varphi_{qs} + \frac{\rho}{\omega_b}\varphi_{ds} \quad (15)$$
$$v_{qs} = r_s i_{0s} + \frac{\rho}{\omega_b}\varphi_{0s}$$

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$$v'_{qr} = r'_r i'_{qr} + \frac{(\omega - \omega_r)}{\omega_b}\varphi'_{dr} + \frac{\rho}{\omega_b}\varphi'_{qr}$$

$$v'_{dr} = r'_r i'_{dr} - \frac{(\omega - \omega_r)}{\omega_b}\varphi'_{qr} + \frac{\rho}{\omega_b}\varphi'_{dr}$$

$$v'_{qr} = r'_r i'_{0r} + \frac{\rho}{\omega_b}\varphi'_{or}$$

4. RESULTS AND DISCUSSION

4.1 Rectifier Output and Harmonic Analysis

The 12-pulse transformer was modeled with a single primary winding and two secondary windings, providing a 30° phase shift between the star and the delta windings. Figures 7-8 show Simulink model and the corresponding secondary voltage waveforms, confirming the correct phase displacement necessary for harmonic cancellation.

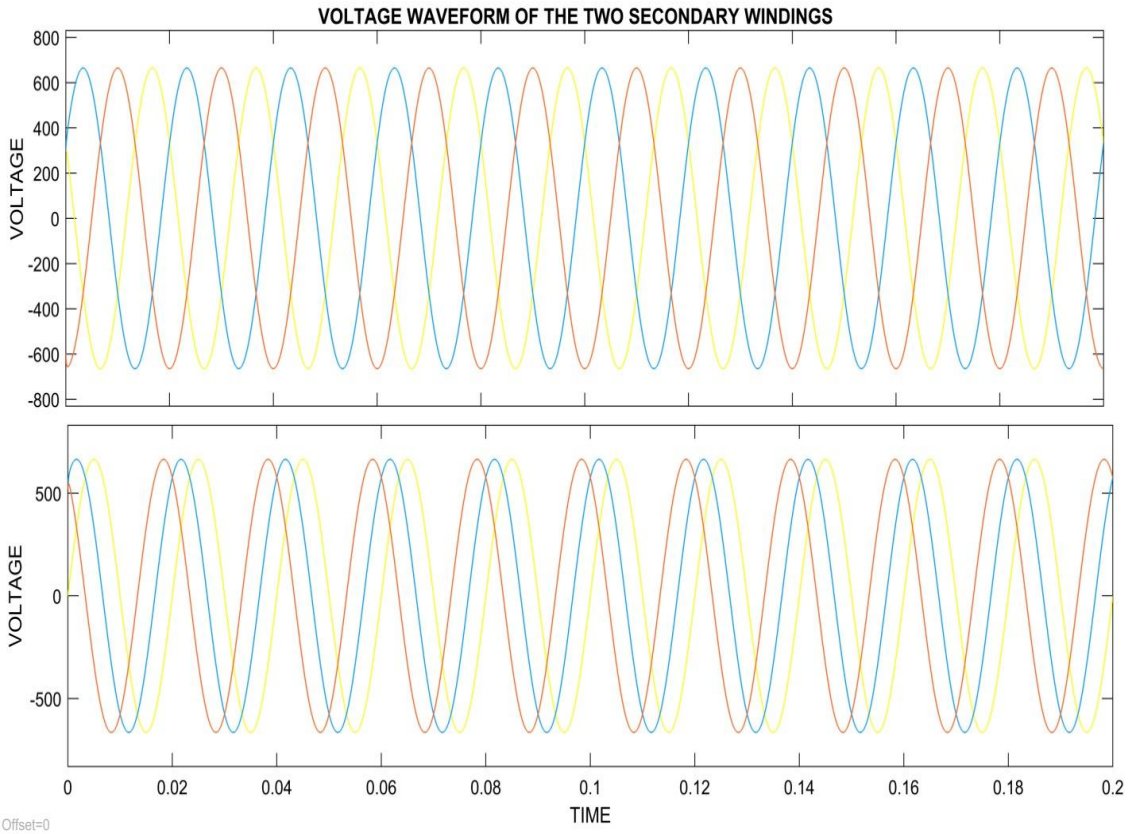

Figure 7 Secondary Voltage Waveform for the Star and Delta

The two secondary windings feed the two 6-pulse diode bridge rectifiers, whose outputs are connected in parallel to form the 12-pulse rectifier system. Figure 8a show how the input phase-to-phase current of the star secondary and the output of the upper 6-pulse rectifier, Figure 8b show how the input phase-to-phase current of the delta secondary and the output of the lower 6-pulse rectifier clearly showing the 30 degree phase shift with respect to the star waveforms, Figure shows how the 12-pulse is generated by the algebraic sum of the two

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output (VDC-01 and VDC-02) to form the output voltage VDC which is connected to the load, and Figure shows the (VDC) output voltage waveform which demonstrates reduced ripple. Maximum (663V) to minimum (640V) ripple voltage of 12-pulse rectifier is 23V compared to any of the 6-pulse rectifier having maximum (663V) to minimum (570V) ripple voltage of 93V.

b

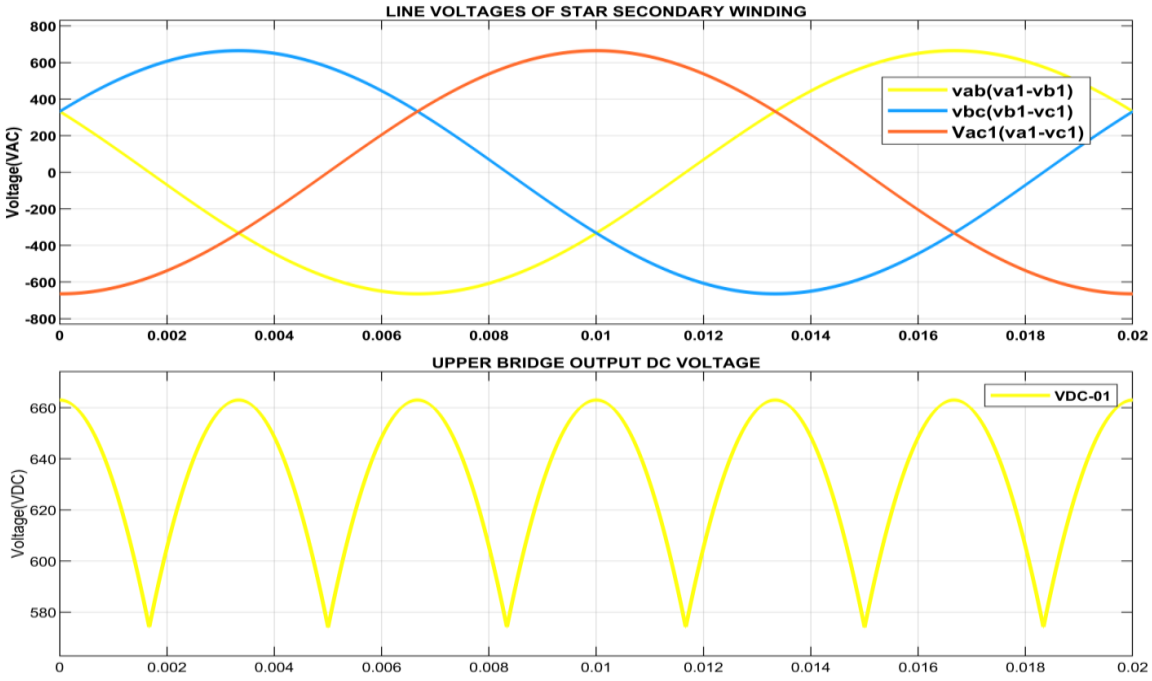

Figure 8a Upper bridge rectifier input AC Voltage and output DC Voltage

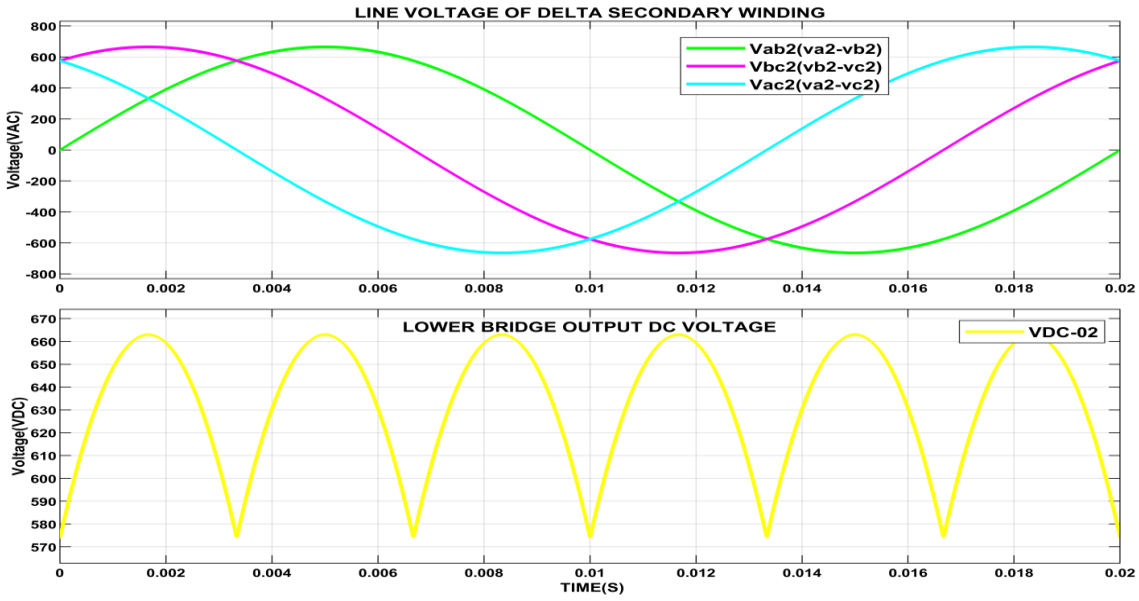

Figure8b Lower bridge rectifier input AC Voltage and output DC Voltage

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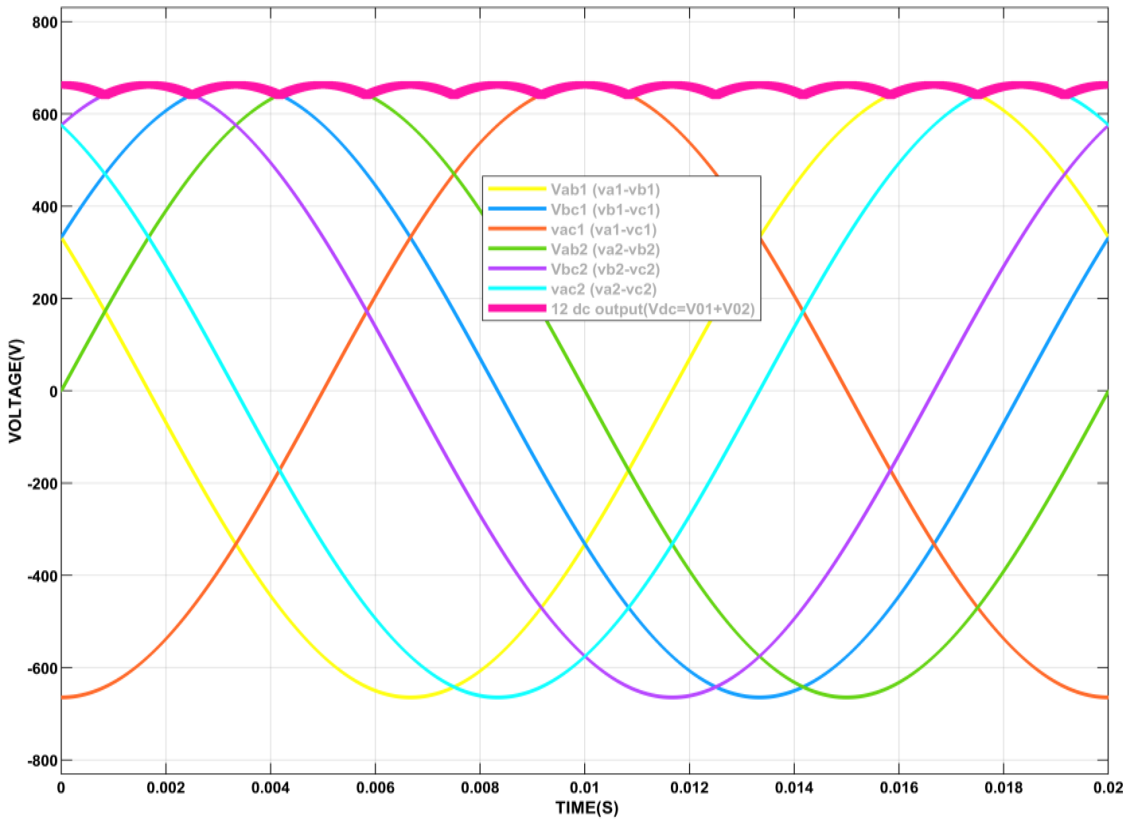

Figure 9: 12 pulse rectifier input AC Voltages and output DC Voltage

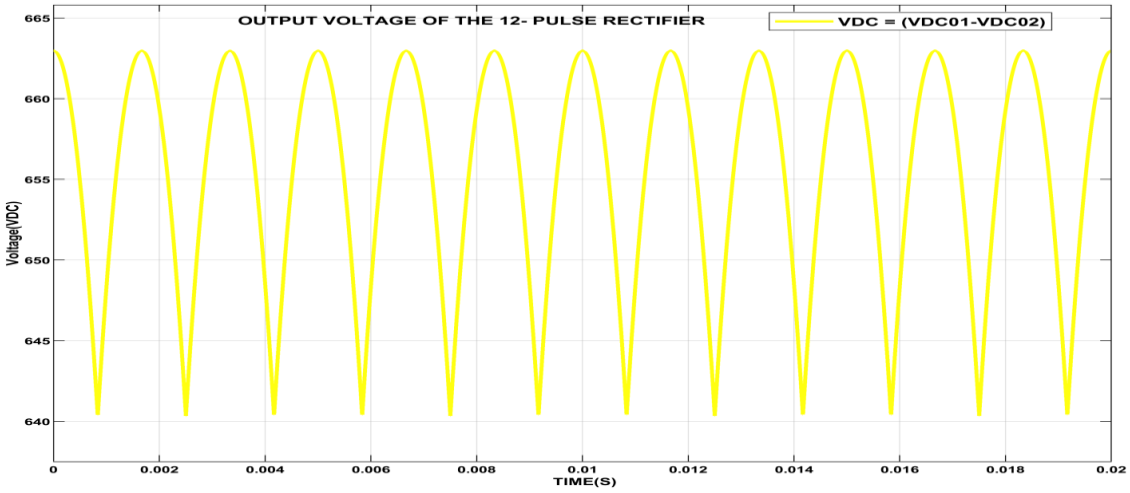

Figure 10: 12-pulse output DC Voltage

Fourier analysis of the output VDC of the rectifier in Figure and Figure reveals significant suppression of the 5th, 7th, 11th, and 13th harmonics. The Total Harmonic Distortion (THD) is reduced from approximately 5.95% (6-pulse) to 1.46% (12-pulse). Harmonic content before filtering for 6-pulse and 12-pulse bridge rectifier as shown in Figure and Figure 12, clearly shows that the ripple voltage for the 12- pulse rectifier actual started from 12 times supply frequency. The rectifier filtered output is shown in Figure 13 when the dc choke inductor and filter capacitor is connected to the output of the rectifier.

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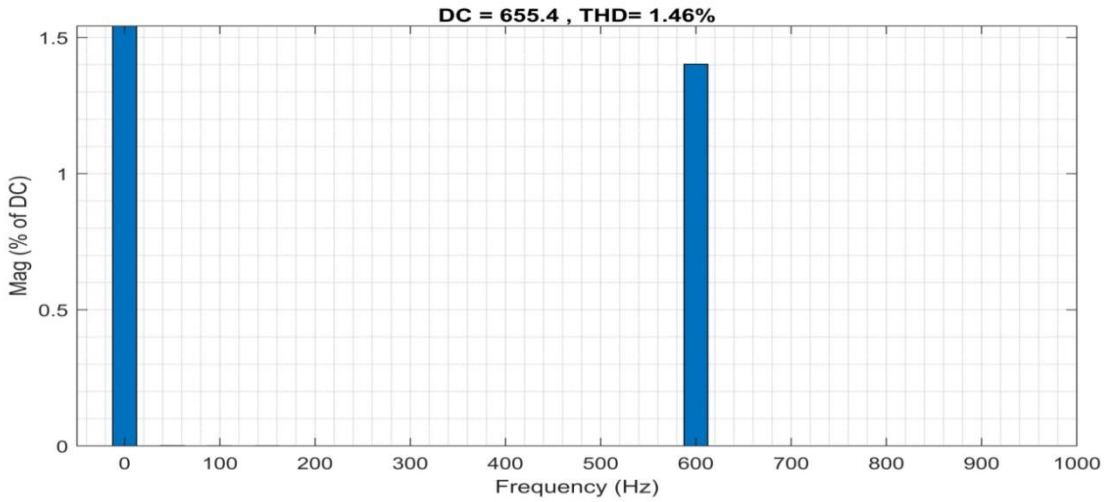

Figure 11: FFT of Input current of 12-pulse rectifier

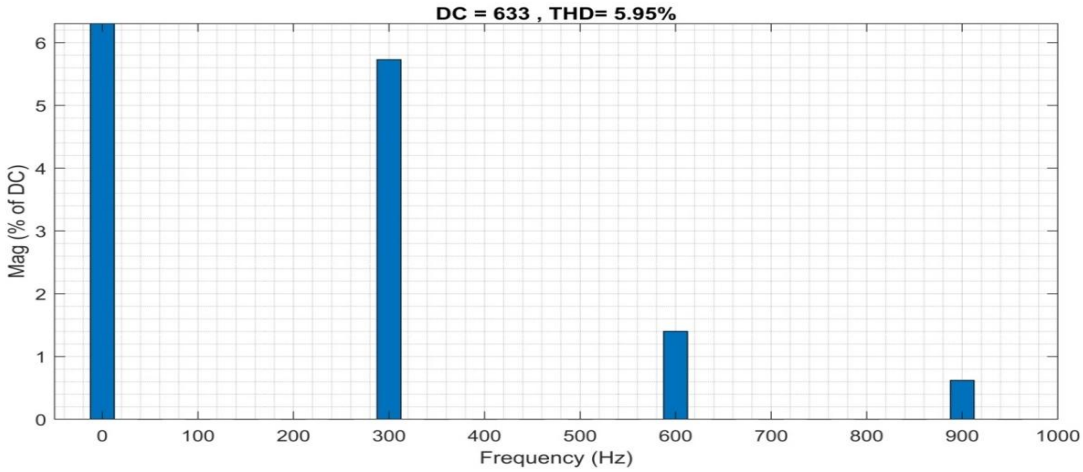

Figure 12: FFT of Input current of 6-pulse rectifier

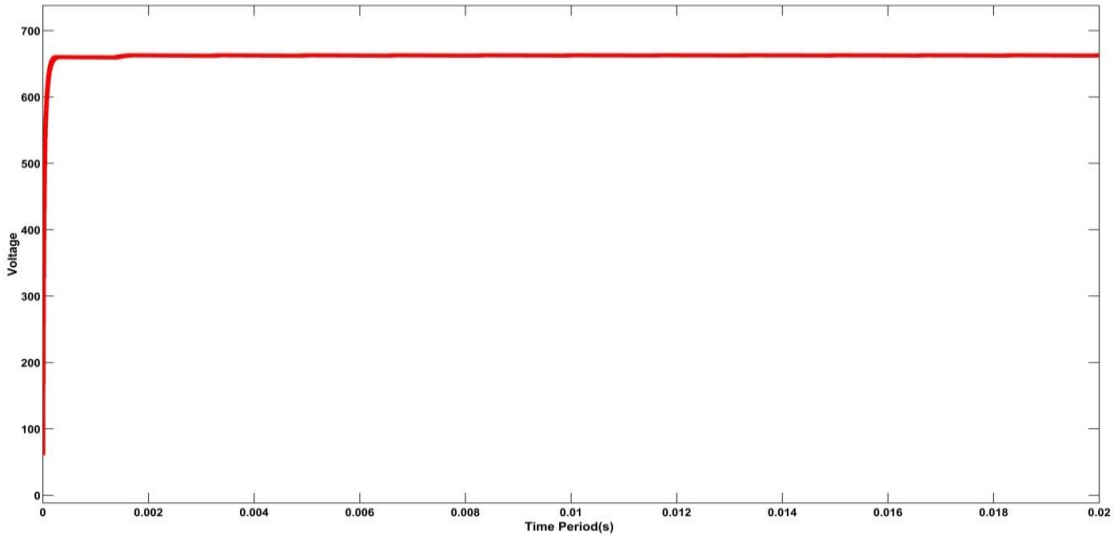

Figure 13 DC Output after DC Choke (Filter

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4.2. Inverter Topology and Simulations:

A 5-level DCMLI was designed using IGBTs, as shown in Figure 5. The inverter was tested under different PWM strategies: Phase Disposition (PD), Phase Opposition Disposition (POD), and Alternate Phase Opposition Disposition (APOD). The modulating signal for the different PWM is for red phase is shown below in Figure 14 using modulating signal of 50 Hz which represent the highest speed and carrier signal of 5 KHz. Figure 15 represents the output of the 5- level diode clamped multilevel inverter phase-to-neutral and line-to-line voltage, from the graph the line voltage is the algebraic sum of the two phase voltages and it shows that the levels for phase-to-neutral are $+\frac{V_{dc}}{2}$, $+\frac{V_{dc}}{4}$, 0, $-\frac{V_{dc}}{4}$, $-\frac{V_{dc}}{2}$, while line-to-line voltage components are: $+Vdc$, $+\frac{V_{dc}}{2}$, 0, $-\frac{V_{dc}}{2}$, $-Vdc$, which demonstrate the required 5-level for this thesis.

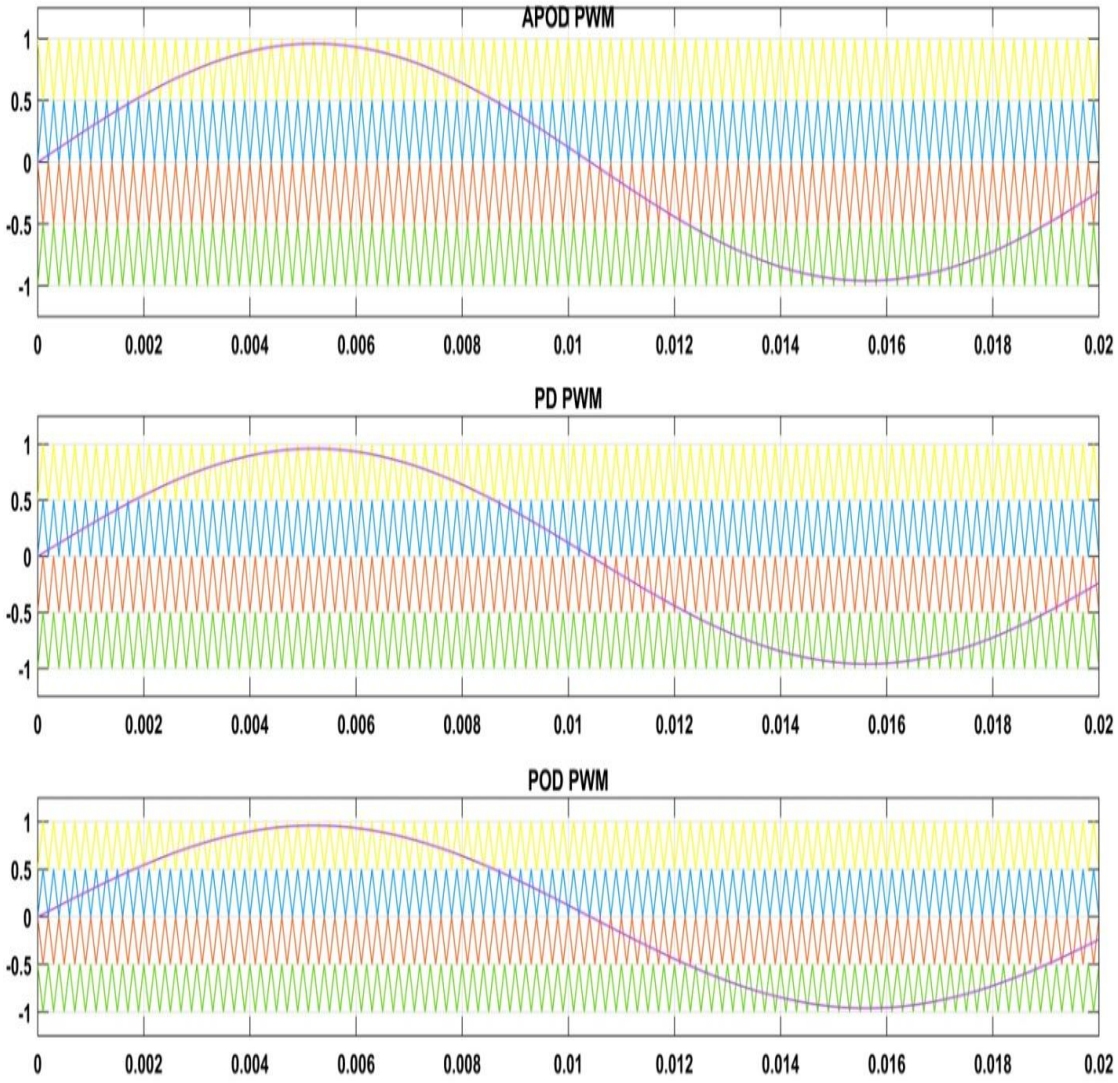

Figure 14: Red Phase Modulation for APOD PD and POD

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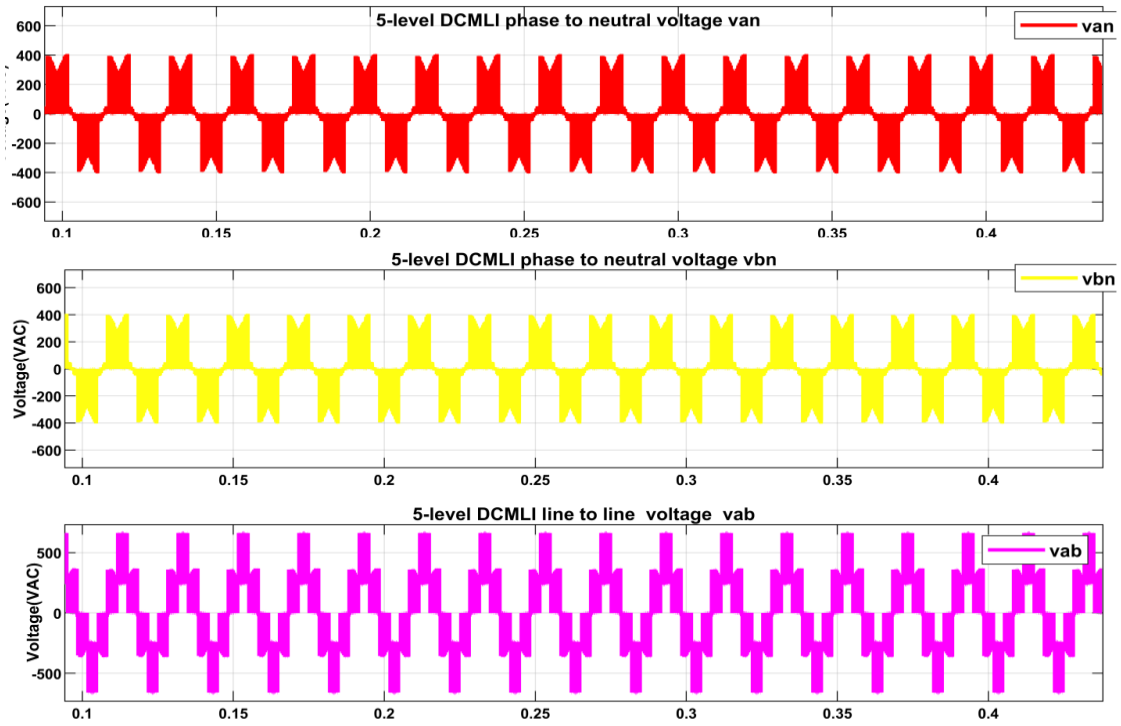

Figure 15 Output Phase And Line Voltage of the 5-Level DCMLI Inverter

Figure 16 display the 3 phase voltages and the performance of the induction motor for different PWM, for PD, POD, and APOD the Voltage levels and the motor performance look very similar but what differs is the THD as show in the FFT analysis of different modulation method

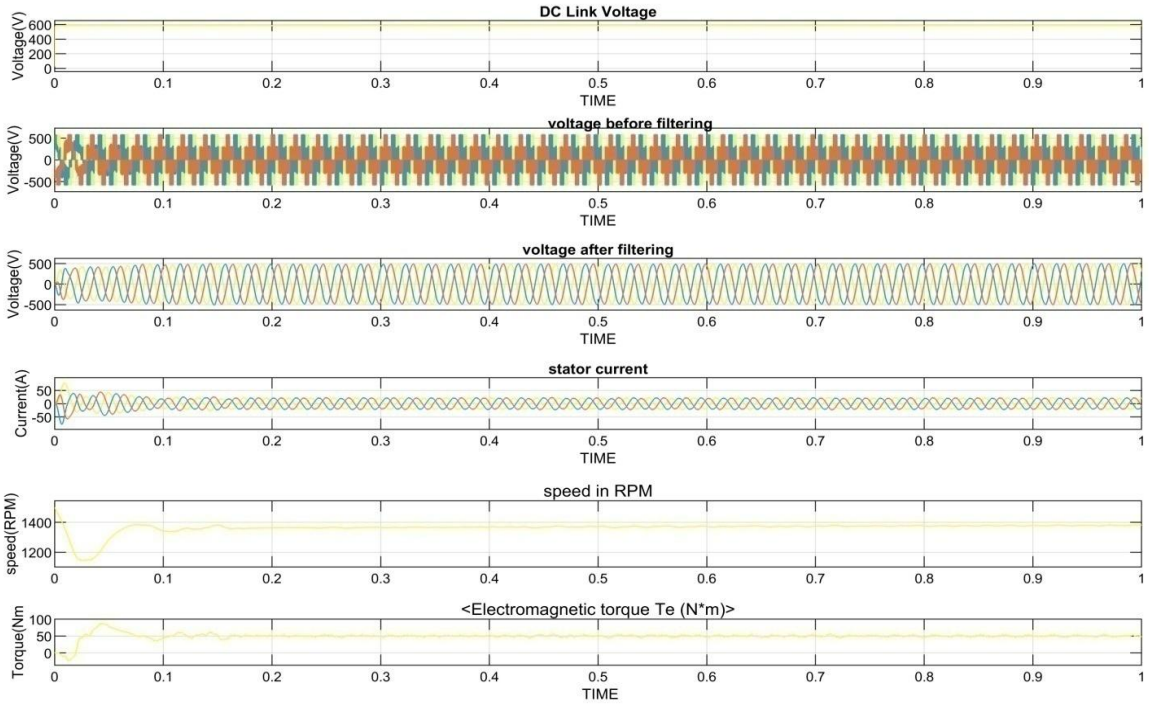

Figure 16 output waveform of the inverter and the motor performance under APOD modulation.

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4.2.1 Harmonic Spectrum and THD for Induction Motor

Harmonic analysis using FFT for all the modulation techniques are shown in, Figure 17, Figure 18, Figure 19Figure , and Figure 20 showing that APOD PWM achieves the lowest THD and at the same time has ability to achieve a good balance between output voltage and current. Total harmonics distortion (THD) among the tested methods, shows that APOD outperformed PD and POD and normal 3-level inverter. For industrial motor control where voltage balancing is an importance factor both in the relay protection programming and the lifespan of the induction motor, low THD is maintained to enhance voltage stability

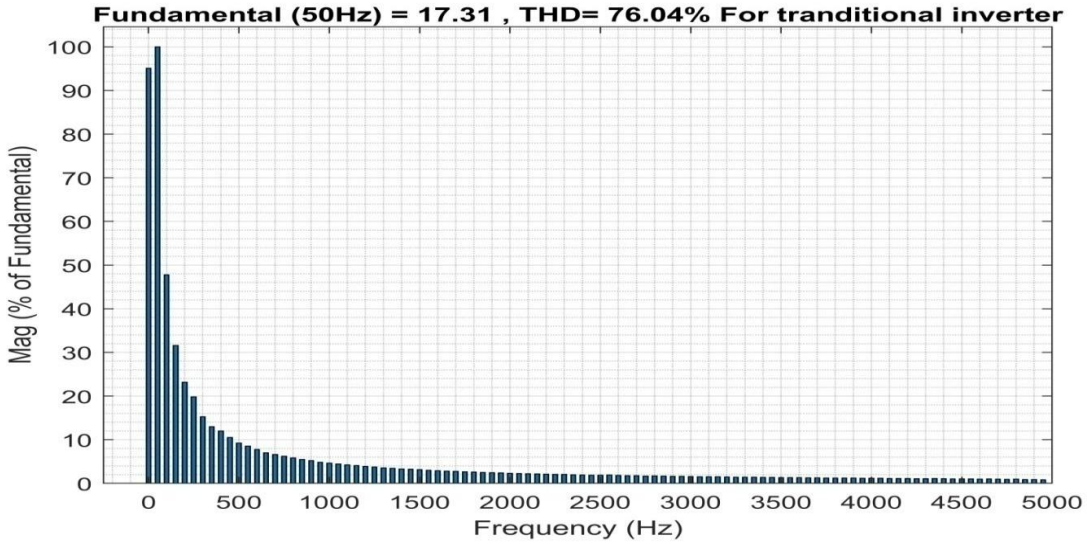

Figure 17 FFT Analysis for Normal Inverter

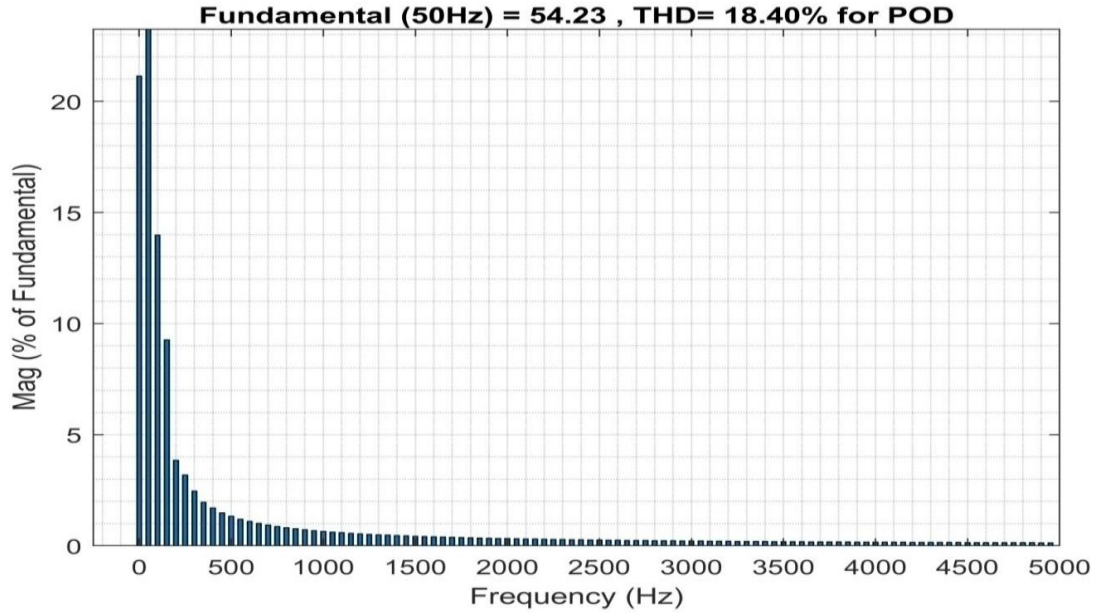

Figure 18: FFT Analysis for 5 levels DCMLI using POD

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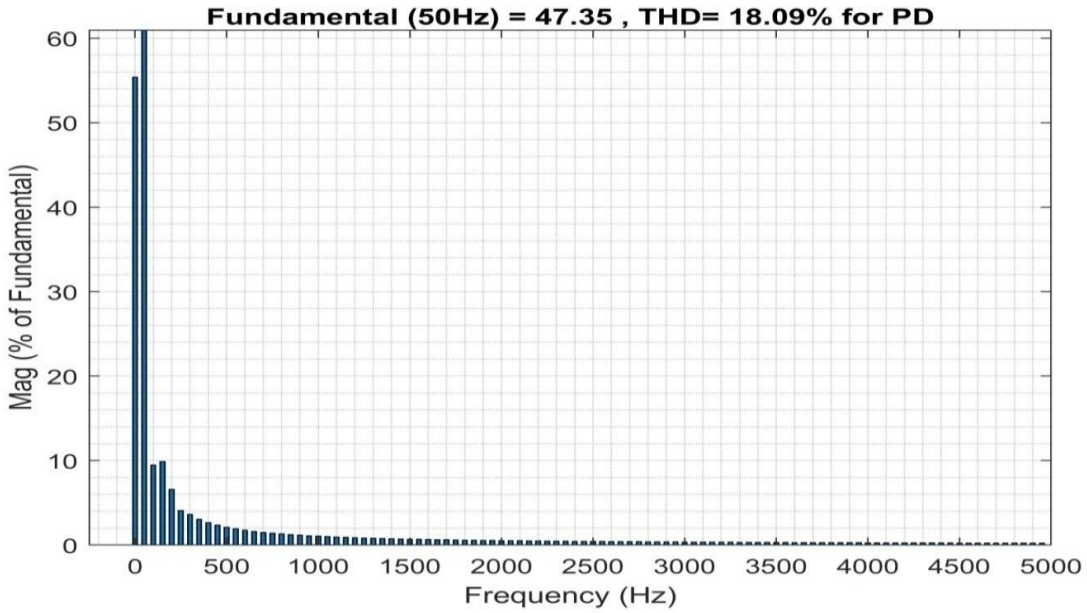

Figure 19. FFT Analysis for 5 levels DCMLI using PD

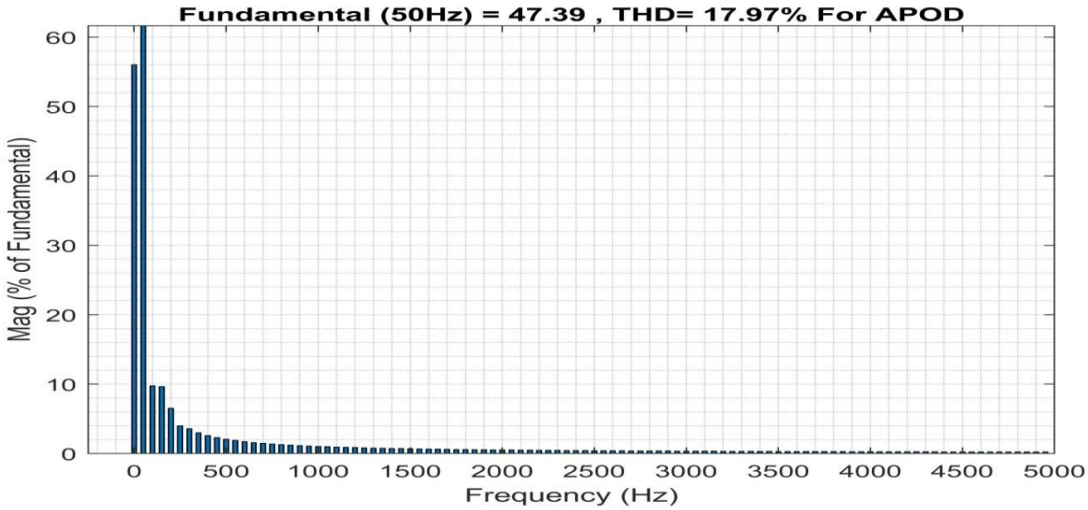

Figure 20 FFT Analysis for 5 levels DCMLI using APOD

4.2.2 Harmonic Spectrum and THD for Input Supply

The Fourier fast transform (FFT) of the input current of the supply when 6-pulse and 12-pulse rectifier is shown in Figure 21 , and Figure 22 , it shows that the THD is reduced from 69.84% to 62.23% this reduction also contribute to the low energy cost, low switching losses and it enhance the voltage stability of the grid.

4.2.3 Harmonic Spectrum and THD for Inverter Output Voltage

The Fourier fast transform (FFT) of the inverter voltage during and after connecting the output filter is shown in Figure 23, and Figure 24 showed that the THD is reduced from 37.45% to 16.37%. Also this reduction also contribute to the low energy cost, low switching losses in inverter MOSFET and rectifier diodes enhances the voltage stability of the grid and reduces harmonics to the induction motor and the grid.

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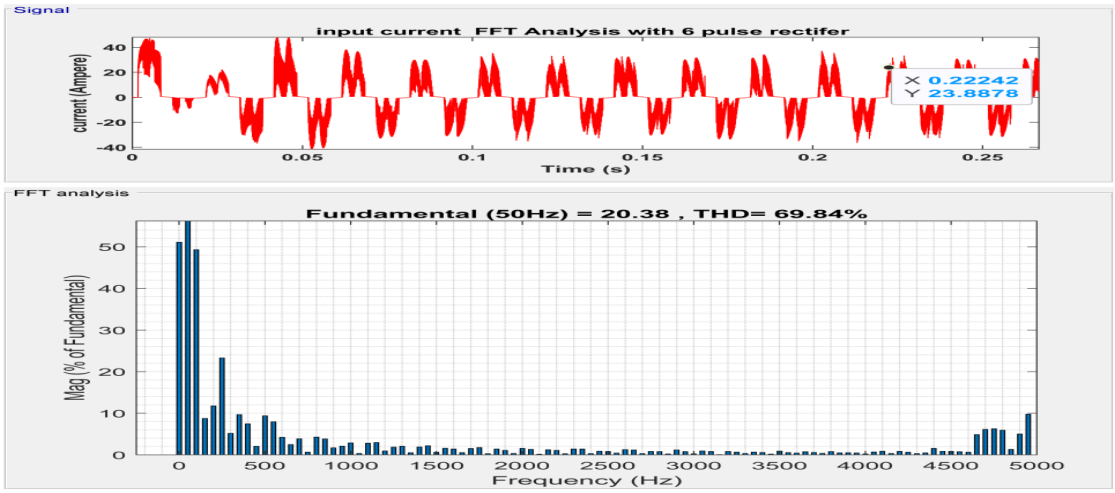

Figure 21: FFT Analysis of input current 6-pulse rectifier

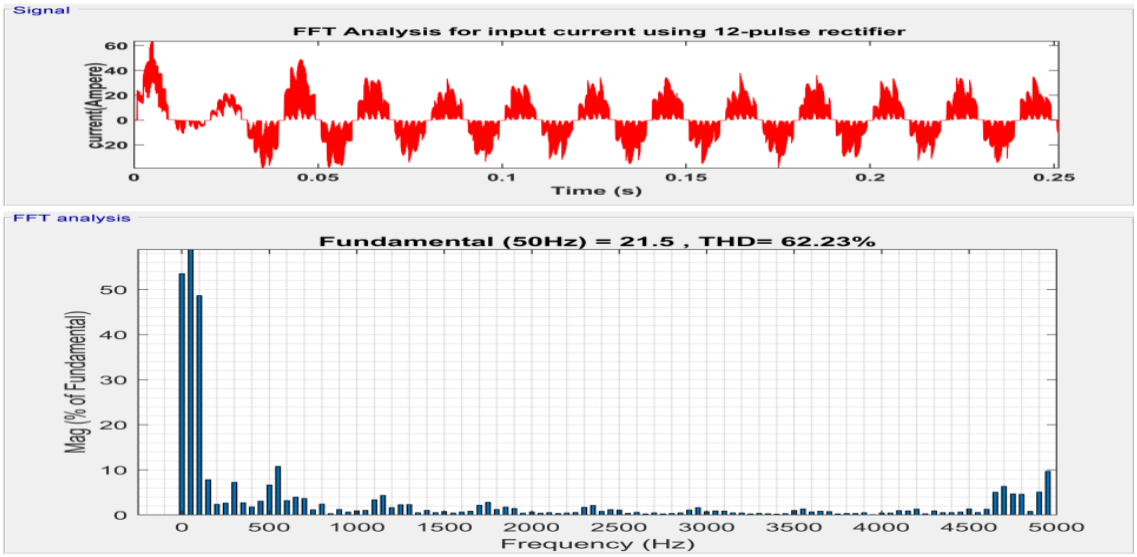

Figure 22: FFT Analysis of input current 12-pulse rectifier

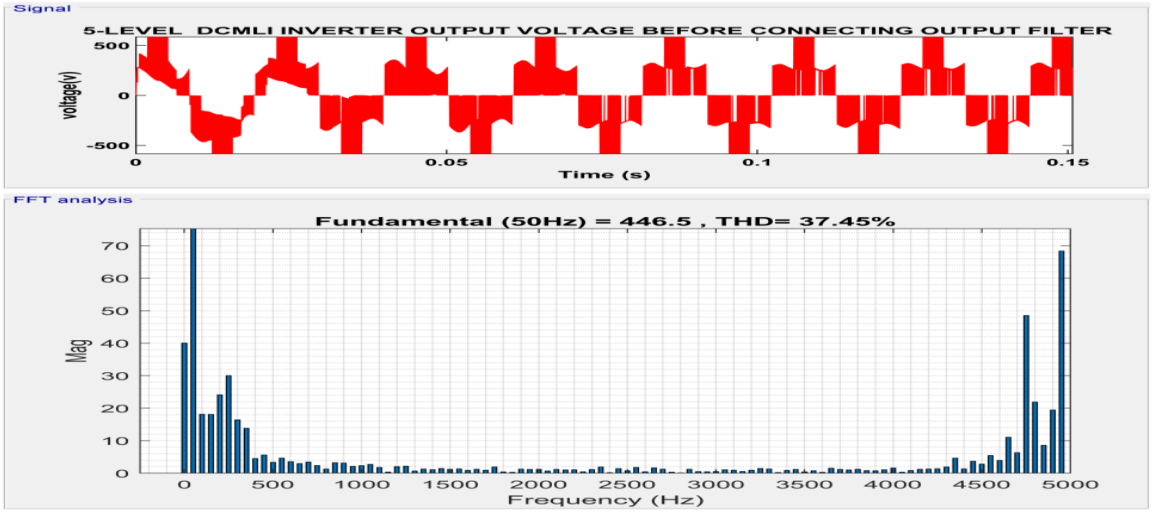

Figure 23 FFT analysis Inverter Output Voltage before filtering

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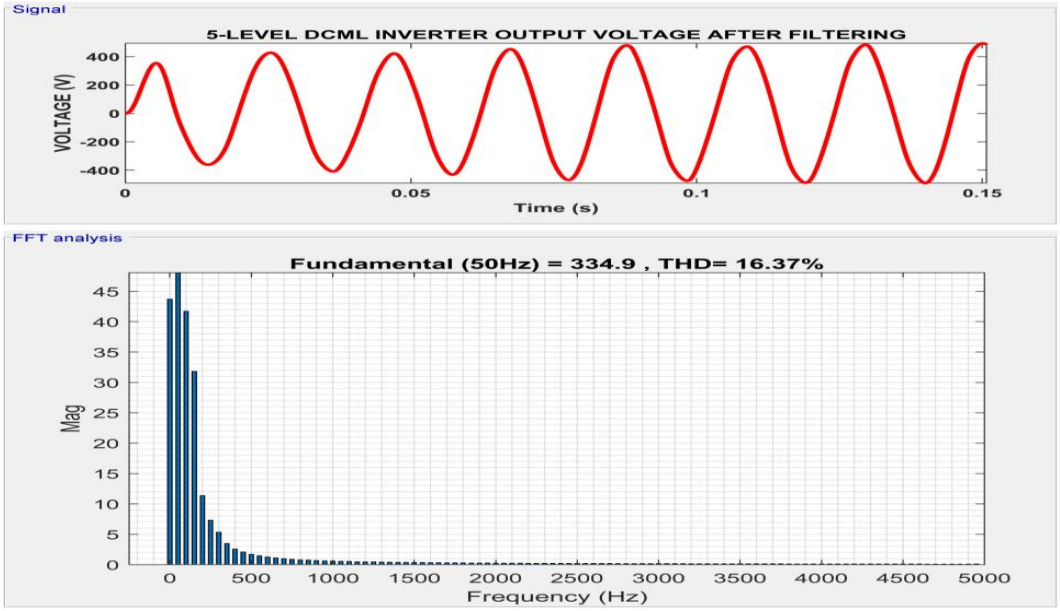

Figure 24 FFT analysis Inverter Output Voltage after filtering

4.2.4 Comparative Analysis

Table 6 summarizes the THD values for each PWM strategy. APOD not only reduces harmonics but also ensures better voltage balancing across inverter capacitors.

Table 6: Comparative value for Different PWM Techniques

	PD	POD	APOD	Normal inverter
Frequency	47.35	54.23	47.39	17.31
THD (%)	18.09	18.40	17.97	76.04

4.2. Harmonic Mitigation Using Passive Output Filters

A passive LC filter was designed and connected at the inverter output. The filter parameters were selected to target dominant harmonics while minimizing losses and phase shift, Figure 23, and. Figure 24 compare the output voltage and Figure 20Figure shows the FFT analysis current of the waveforms before and after filtering. The filtered waveforms are smoother and more sinusoidal, with reduced high-frequency content. Figure 21, Figure 22, and Figure presents the harmonic spectrum of the output current for different PWM. The THD drops from about 61.1% (unfiltered) to 17.49% (filtered) for APOD PWM, and also the inverter voltage THD from 37.45% to 16.37% confirming the filter's effectiveness. The smoother output reduces torque ripple and motor heating, enhancing reliability and efficiency. The passive filter, in conjunction with the 12-pulse rectifier and multilevel inverter, achieves industry-standard power quality.

5. CONCLUSION

This study modeled and analyzed a 12-pulse rectifier integrated with a five-level diode-clamped multilevel inverter for induction motor drives. The simulation results indicated that harmonic performance, power factor, and energy optimization of the proposed system is significantly better than that of a conventional six-pulse VFD. Among the PWM techniques analyzed, the APOD strategy provided the lowest THD and the best dynamic performance.

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Using a DCMLI and a 12-pulse rectifier is a suitable solution for industrial motor drives that requires high efficiency and good power quality.

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