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Development of DC-Biased Enhanced Unipolar Modulation Topology for DC -AC Power Converter-fed Single-phase Induction Motor

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Abstract

This work presents development of DC-biased enhanced unipolar modulation topology for DC -AC power converter-fed single-phase induction motor. The system is modeled and simulated in MATLAB/Simulink environment to single-phase induction motor. It presents a comparative analysis on the output parameters with the inverter fed of the same induction motor. The proposed approach on triggering multilevel DC-AC power switches is based on an enhanced unipolar modulation scheme. This scheme consists of two modulating signals phase-shifted at180 degrees from each other and two DC-biased triangular carriers that were combined to generate firing signals. The outcome of the comparison between the carriers and reference sinewave produces switching signals used for firing the switches of conventional single-phase full bridge diode-clamped multilevel inverter. This scheme was designed to reduce the number of carrier waves and minimize the overall modulation circuit to obtain a stabilized output voltage waveforms. Unlike the conventional multicarrier sinusoidal pulse width modulation that uses four triangular waves and one modulating sine wave for the same inverter type, the proposed system has only two triangular waves and two reference sinewaves. This means that the proposed system has total of 4 while conventional modulations have 5. The proposed modulation scheme has advantages of reduced number of components therefore reduced cost of implementation and can easily be packaged. It also possesses all its carrier waves operating in continuous current mode which makes it unique from other multicarrier and other related modulation schemes. Output voltage of 200V and current of 20A with corresponding total harmonic distortions of 0.4075% and 0.2509% at Frequency of 50Hz with the output power of 4kw were the results obtained from the simulation and that was validated with experimental prototype. And the practical wave forms were displayed.

Keywords: *DC-biased, DC-AC Power Converter, Enhanced, Modulation, Induction Motor, Unipolar.*

1. INTRODUCTION

The demand for high power equipment in industries has recently gained much attention from researchers all over the globe. Multilevel inverter is one of the proposed power inverters to meet the power handling capacity and has drawn concern on energy control due to their merit of high-power applications with low harmonics.

Power inverter is said to be power electronics device that converts DC power through the use of power switches to AC power at desired voltage and frequency. Multilevel inverter on the other hand is a power inverter that ranges from 3-level and above and has improved power quality, good efficiency and maintenance. [1]-[9]

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It ranges from different topologies among others are, Diode Clamp or Neutral point inverter (DC-MLI), Flying Capacitor multilevel inverter (FC-MLI), Cascaded or H-bridge inverter and Hybrid inverters. These find its applications in Flexible AC transmission system, Induction Machine and Motor drives, Interface of renewable energy sources to mention a few.[10]-[12]

Some topologies like DC-MLI and FC-MLI have disadvantage of voltage imbalance on input capacitors that aggravates beyond simulation time of 0.1 seconds if not compensated with external circuitry as already mentioned in [5] and seen in [13]-[16].

Remarkable modulations scheme for multilevel inverters aimed at resolving key number of issues such as Capacitor voltage imbalance, high total harmonic distortion of output voltage and high EMI have been published by many Authors with their boons and banes.

The various pulse width modulation schemes are: sinusoidal pulse width modulation (SPWM) which has two different strategies, unipolar and bipolar SPWM [17], sixty-Degree pulse width modulation, Trapezoidal pulse width modulation (TPWM), Third Harmonic injected pulse width modulation (THIPWM), Space Vector pulse width modulation (SVPWM) and selective harmonic elimination pulse width modulation (SHEPWM).[18]-[21].

In this research, an DC-biased Enhanced unipolar modulation topology was developed and optimized to obtain full range capacitor balance in 5 level line to line output voltage Diode–clamp multilevel inverter.

This is based on enhanced unipolar multicarrier PWM topology and is distinguished from other modulation topologies in that;

i. It has DC-biased carrier waveforms that enables it to operate in continuous current mode
ii. The triggering signals comprises of compress and decompress regions that suppresses higher and lower order harmonic, therefore maintaining low THD.
iii. It has lower circuit component counts of modulation circuit scheme and its experimental prototype

2. MATERIALS AND METHODOLOGY

The power circuit of Fig 1 was built with eight insulated gate bipolar transistors, (IGBT), two capacitors that divide the input dc voltage, four high quality rectifier diodes, connecting lines, single-phase induction motor load and DC power source.

Modeling, simulation and experimentation were adopted in this work. For a complete cycle of operation of Fig 1, five output voltages are generated as: $v_o = 0v$, v_s, $v_s/2$, $-v_s$ and $-v_s/2$. 0v is generated as a result of transition from positive half cycle to negative half cycle whereas v_s, $v_s/2$ and $-v_s$, $-v_s/2$ are generated during positive and negative half cycle respectively.

The proposed system converts the electrical energy to mechanical energy. Digital oscilloscope and Analog oscilloscope were used to view the practical waveforms of the system outputs. The oscilloscopes were used because we are not the owners. We borrowed them to use. Any available one, was what we were using during the research experimentation.

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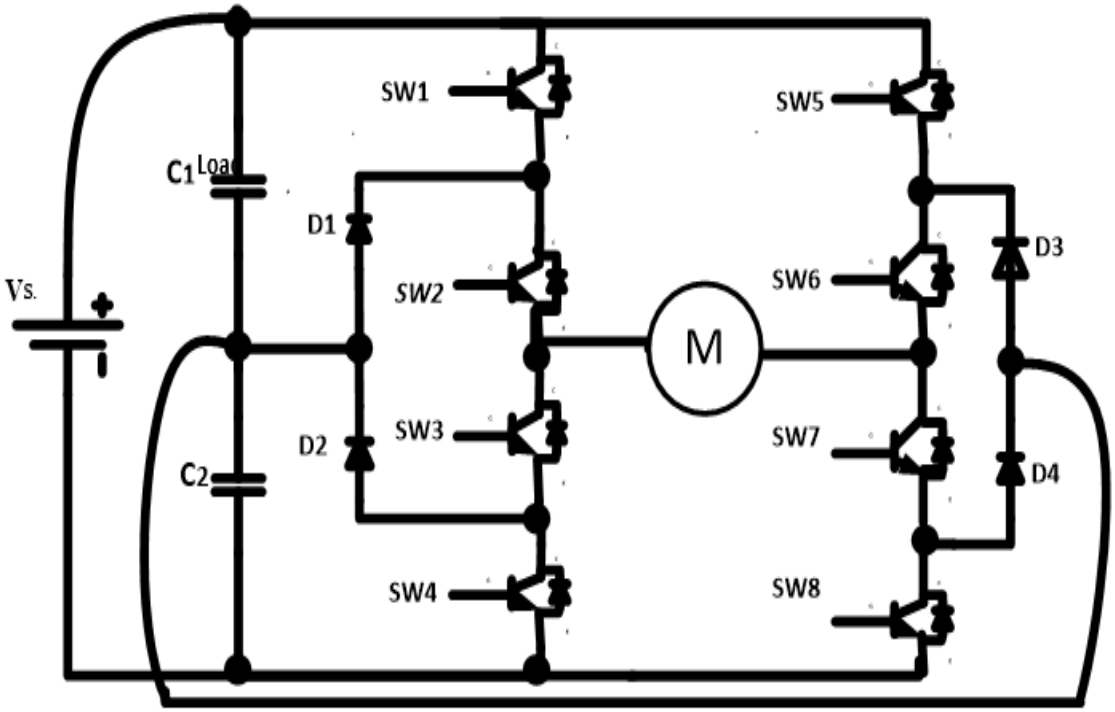

Figure 1: Conventional five level full Bridge DC-MLI [5]

The eight switching states for Fig 1 are shown in Table 1 as well as the corresponding output voltage for each switching sequence.

Table 1: Switching state for the five levels Full Bridge DC-MLI

SW8	SW1	SW2	SW3	SW4	SW5	SW6	SW7	Vo
1=ON	1=ON	1=ON	0=OFF	0=OFF	0=OFF	0=OFF	1=ON	Vs
1=ON	0=OFF	1=ON	1=ON	0=OFF	0=OFF	0=OFF	1=ON	Vs/2
1=ON	0=OFF	0=OFF	1=ON	1=ON	0=OFF	0=OFF	1=ON	0
1=ON	0=OFF	0=OFF	1=ON	1=ON	0=OFF	1=ON	1=ON	-Vs/2
1=ON	0=OFF	1=ON	1=ON	0=OFF	0=OFF	0=OFF	1=ON	-Vs

3. DC-BIASED ENHANCED UNIPOLAR MODULATION TOPOLOGY

The block diagram realization of the modulation scheme is displayed in Fig.2a. Figure 2a is modulation technique proposed for producing triggering signals for switching the Diode clamp MLI of Figure 1.

The proposed modulation was developed using two modulating signals $V_{ref.1}$,$V_{ref.2}$ which are phase shifted by 180 degree and two carrier signals $V_{tr.1}$, $V_{tr.2}$ that are dc-offset as in Figure 2b. The switching frequency of the triangular wave is greater than the frequency of the reference sinewave. This scheme helps further in mitigation of both low order and high order harmonics unlike the conventional schemes that are only in one sided mitigation. The micro-controller is further utilized to further process the pulses. The TLP 350IC drivers were used to isolate, buffer and strengthen the triggering signals.

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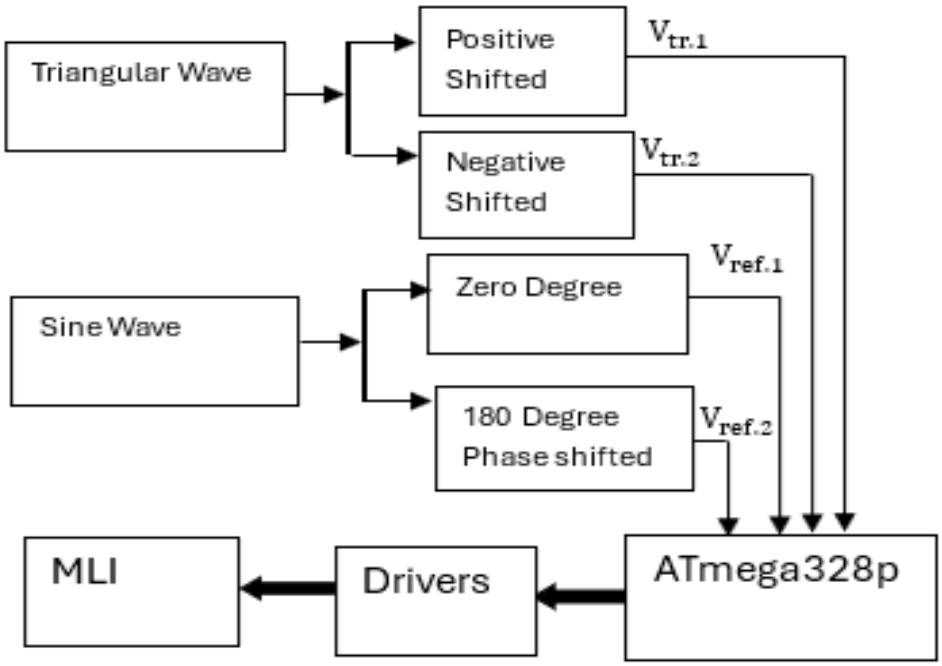

Figure 2b: DC-Offset Enhanced unipolar modulation topology

Figure 2b shows a typical illustrative representation of the DC-biased enhanced unipolar modulation scheme. It consists of two DC-biased triangular waves (Vtr.1 & Vtr.2) and two reference sinewave forms (Vref.1 & Vref.2). The DC-biased triangular waves are completely of the zero-axis. And for that reason, it operates in continuous conduction mode.

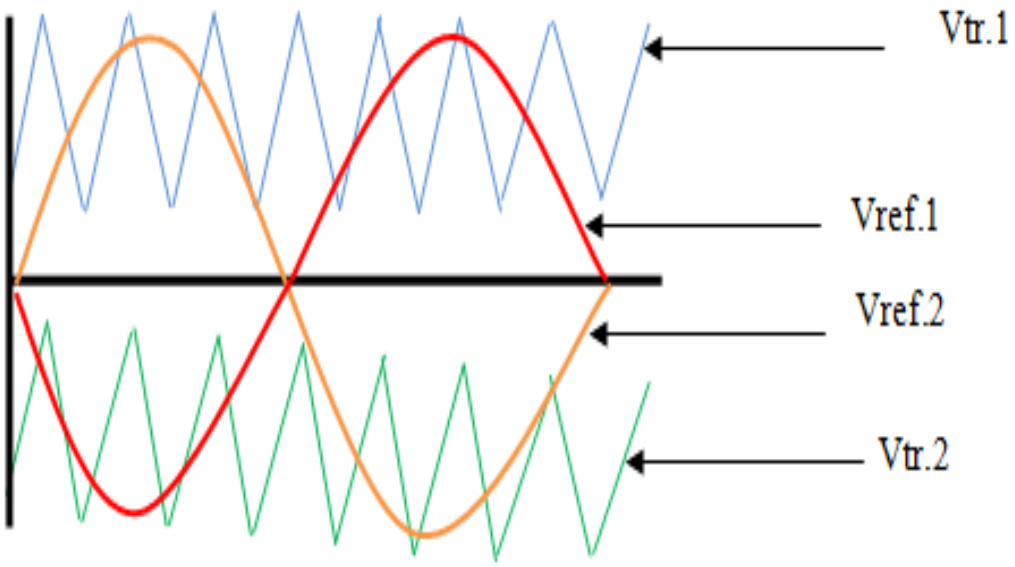

Figure 2b: Carriers and modulating signals

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4. MATHEMATICAL ANALYSIS OF THE DC-BIASED ENHANCED UNIPOLAR MODULATION SCHEME

The mathematical derivation of the carrier signals of Figure 3 is thus, Considering the Non-Inverting Signal of the Op- amp A (comparator) in Figure 3

$$V_{in} = \frac{V_{01}}{R_2} + \frac{V_{02}}{R_3} \tag{1}$$

and

$$V_{02} = \frac{(R_2+R_3)}{R_2} V_{in} - \frac{R_3}{R_2} V_{01} \tag{2}$$

The output swing of the comparator is assumed to be symmetrical about zero ($\pm V_{01}$) whether it is related to the supply voltage or not [34]. The circuit switches when V_{in} get to zero and this condition defined the peak to peak (P-P) output voltage $V_{02} - (-V_{02})$ in relatives to P-P swing of op-amp B. From equation (2) the peak to peak output voltage is given in equation (3)

$$V_{02}(P-P) = -\frac{R_3}{R_2} 2V_{01} \tag{3}$$

Considering the Non-Inverting Signal of the Op- amp B (integrator), The output voltage with respect to time (t) is given in equation (4) and this time is the time taken by the output to swing from $-V_{02}$ to $+V_{02}$ which is equal to half of the period (T/2)

$$V_{02} = -\frac{V_{01}}{R_4 C} t \tag{4}$$

The step change in V_{in} caused by V_{01} must be equal to the height of the slope change caused by V_{02}

Therefore,

$$-\frac{R_3}{R_2} 2V_{01} = -\frac{V_{01}}{R_4 C} t \tag{5}$$

From equation (5) t is realized to be,

$$t = \frac{R_3}{R_2} \times 2R_4 C \tag{6}$$

Where, t is time taken for Op Amp to be on/off

The period T is 2t, therefore,

$$T = \frac{R_3}{R_2} \times 4R_4 C \tag{7}$$

And the frequency

$$f_1 = \frac{R_2}{R_3} \times \frac{1}{4R_4 C} \tag{8}$$

The matlab entry for Vtr. 1 and Vtr. 2 is given as:

$$Vtr.1 = \begin{bmatrix} 0 & \frac{1}{4f_1} & \frac{1}{2f_1} & \frac{3}{4f_1} & \frac{1}{f_1} \\ V_a & 2V_a & 3V_a & 2V_a & V_a \end{bmatrix} \tag{9}$$

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$$Vtr.2 = \begin{bmatrix} 0 & \frac{1}{4f_1} & \frac{1}{2f_1} & \frac{3}{4f_1} & \frac{1}{f_1} \\ -3V_a & -2V_a & -V_a & -2V_a & -3V_a \end{bmatrix} \quad (10)$$

Where f_1 and V_a represent the switching of carrier frequency and amplitude voltage of the carrier.

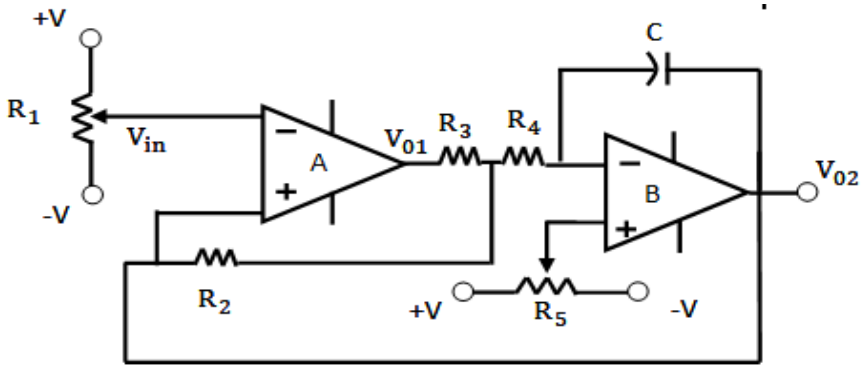

Figure 3: Designed carrier Signals

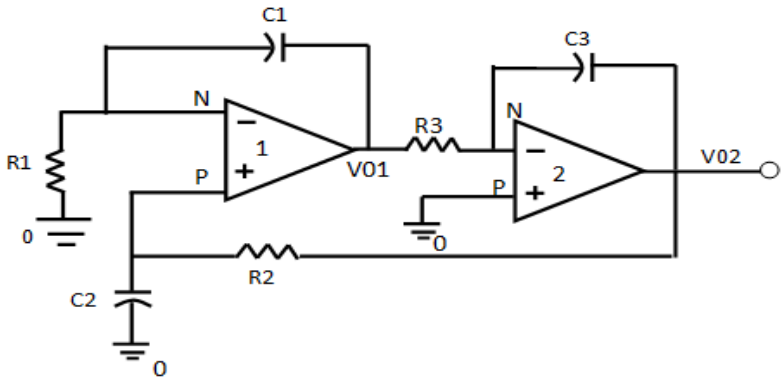

Figure 4: Designed modulating Signals

Considering operational Amplifier A in Figure 4

At the inverting terminal

$$\frac{-V_N}{R_1} = \left(\frac{V_N - V_{01}}{Z_{C1}}\right) \quad (11)$$

$$V_N = \frac{R_1 \times V_{01}}{Z_{C1} + R_1} \quad (12)$$

At non-inverting terminal

$$\frac{0 - V_P}{Z_{C2}} + \left(\frac{0 - V_{02}}{Z_{C2} + R_2}\right) = 0 \quad (13)$$

$$V_P = -\frac{V_{02} \times Z_{C2}}{Z_{C2} + R_2} \quad (14)$$

Where V_N and V_P are voltages at inverting and non-inverting terminals respectively, Z_{C1}, Z_{C2} and Z_{C3} are impedances of C1, C2 and C3. The input voltage for inverting and non-inverting terminals of Op-amp is equal

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So

$$\frac{R_1 \times V_{01}}{Z_{C1}+R_1} = -\frac{V_{02} \times Z_{C2}}{Z_{C2}+R_2} \quad (15)$$

And

$$V01 = -V02 \times ZC1 \times ZC2 + R1 \times ZC2 R1 \times R2 + R2 \times ZC2 \; t = \frac{R_3}{R_2} \times 2R_4C \quad (16)$$

Considering the operational amplifier B,

$$\frac{V_{01}-V_N}{R_3} = \frac{V_N - V_{02}}{Z_{C3}} \quad (17)$$

$$V_N = \frac{V_{01} \times Z_{C3} + R_3 V_{02}}{Z_{C3}+R_3} \quad (18)$$

And $V_P = 0$.

Therefore

$$V_{01} \times Z_{C3} + R_3 \times V_{02} = 0 \quad (19)$$

Substituting equation (16) for V_{01} in (19) equation (20) emerges as;

$$Z_{C1} \times Z_{C2} \times Z_{C3} + R_1 \times Z_{C2} \times Z_{C3} = R_1 \times R_2 \times R_3 + Z_{C2} \times R_1 \times R_3 \quad (20)$$

For a stable reference signal, the capacitors in the circuit of Figure 4 is assigned with the same value C and $R_1 = R_2$. So equation (20) becomes

$$Z_C^3 + Z_C^2 \times R_1 - Z_C \times R_1 \times R_3 - R_1 \times R_1 \times R_3 = 0 \quad (21)$$

And

$$(Z_C + R_1)(Z_C^2 - R_1 \times R_3) = 0 \quad (22)$$

As the resistance cannot be negative

$$Z_C = \pm\sqrt{R_1 \times R_3} \quad (23)$$

Therefore,

$$\frac{1}{2\pi f_2 C} = \sqrt{R_1 \times R_3} \quad (24)$$

And

$$f_2 = \frac{1}{2\pi C\sqrt{R_1 \times R_3}} \quad (25)$$

The Vref.1 and Vref.2 are expressed as in equations (26) and (27)

$$Vref.1 = V_m \left[cos\frac{\pi}{2} \cos 2\pi f_2 t + \sin\frac{\pi}{2} \sin 2\pi f_2 t\right] \quad (26)$$

$$Vref.2 = V_m \left[cos\frac{\pi}{2} \cos 2\pi f_2 t - \sin\frac{\pi}{2} \sin 2\pi f_2 t\right] \quad (27)$$

Where f_2 , is the frequency of modulating (reference) signal in Hz, V_m and $(2\pi f_2 t)$ are the peak voltage of the modulating signal and the phase angle. The frequency modulation, M_f and Amplitude modulation $M_a$of the research system are expressed as in equations 28 and 29

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$$M_f = \frac{f_1}{f_2} \quad (28)$$

$$M_a = \frac{2A_m}{(m-3)A_c} \quad (29)$$

Where, A_m is the amplitude of the modulating signals, A_c is the amplitude of the carrier signals and m is the number of level of MLI

The duty cycle is given as;

$$D = 0.5 + 0.5\left[cos\frac{\pi}{2}\cos 2\pi f_2 t + \sin\frac{\pi}{2}\sin 2\pi f_2 t\right] \quad (30)$$

5. SINGLE-PHASE INDUCTION MOTOR (SPIM) MODEL AND CONTROL AND

The output AC voltage obtained from MLI can be controlled in both magnitude and frequency (voltage/frequency). The controlled AC output voltage is fed to the induction motor drive. When the power switches are **ON**, current flows from the AC bus to the motor windings which are highly inductive in nature; these hold electric energy in the form of current which need to be dissipated while switches are **OFF,** through the freewheeling diodes which are connected across the switches.

The V/f control method permits the user to control the speed of an induction motor at different rates. For continuously variable speed operation, the output frequency of multilevel inverter must be varied. The applied voltage to the motor must also be varied in linear proportion to the supply frequency to maintain constant motor flux.

This is achieved by tuning the duty ratio of the control modulation scheme.

$$V_{qs} = r_{qs} I_{qs} + p\Psi_{qs} \quad (31)$$

$$V'_{ds} = r'_{ds} I'_{ds} + p\Psi'_{ds} \quad (32)$$

$$V'_{qr} = r'_{qr} I'_{qr} + p\Psi'_{qr} - \omega_r \Psi'_{dr} \quad (33)$$

$$V'_{dr} = r'_{dr} I'_{dr} + p\Psi'_{dr} + \omega_r \Psi'_{qr} \quad (34)$$

Flux Linkage Equation can be deduced as

$$\Psi_{qs} = L_{qs} I_{qs} + L_{mq}(I_{qs} + I'_{qr}) \quad (35)$$

$$\Psi'_{qr} = L'_{qr} I'_{qr} + L_{mq}(I_{qs} + I'_{qr}) \quad (36)$$

$$\Psi'_{ds} = L'_{ds} I'_{ds} + L_{md}(I_{ds} + I'_{dr}) \quad (37)$$

$$\Psi'_{dr} = L'_{dr} I'_{dr} + L_{md}(I_{ds} + I'_{dr}) \quad (38)$$

The Electromagnetic Torque Equations are

$$T_e = \frac{P}{2}(L_{mq})(I_{qs} I'_{dr} - I'_{ds} I'_{qr}) \quad (39)$$

$$J\left(\frac{2}{P}\right) p\omega_r = T_e - T_L \quad (40)$$

The speed of the motor is deduced from equation (40) as follow:

$$\omega_r = \frac{T_e - T_L}{J\left(\frac{2}{P}\right)p} \quad (41)$$

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6. MATLAB/SIMULINK MODEL, SIMULATION RESULTS AND DISCUSSION

The power circuit model in Figure 5 is the MATLAB/Simulink model with the proposed modulation topology. The spectral characteristics of output voltage and current as shown in the simulated MATLAB model indicated that at fundamental frequency of 50Hz and maximum voltage of 200V and current of 20A, the system output voltage has the total harmonic distortion (THD) of 0.4075% and that of current is 0.2509%. It is evidence that current is lagging the voltage under the motor load.

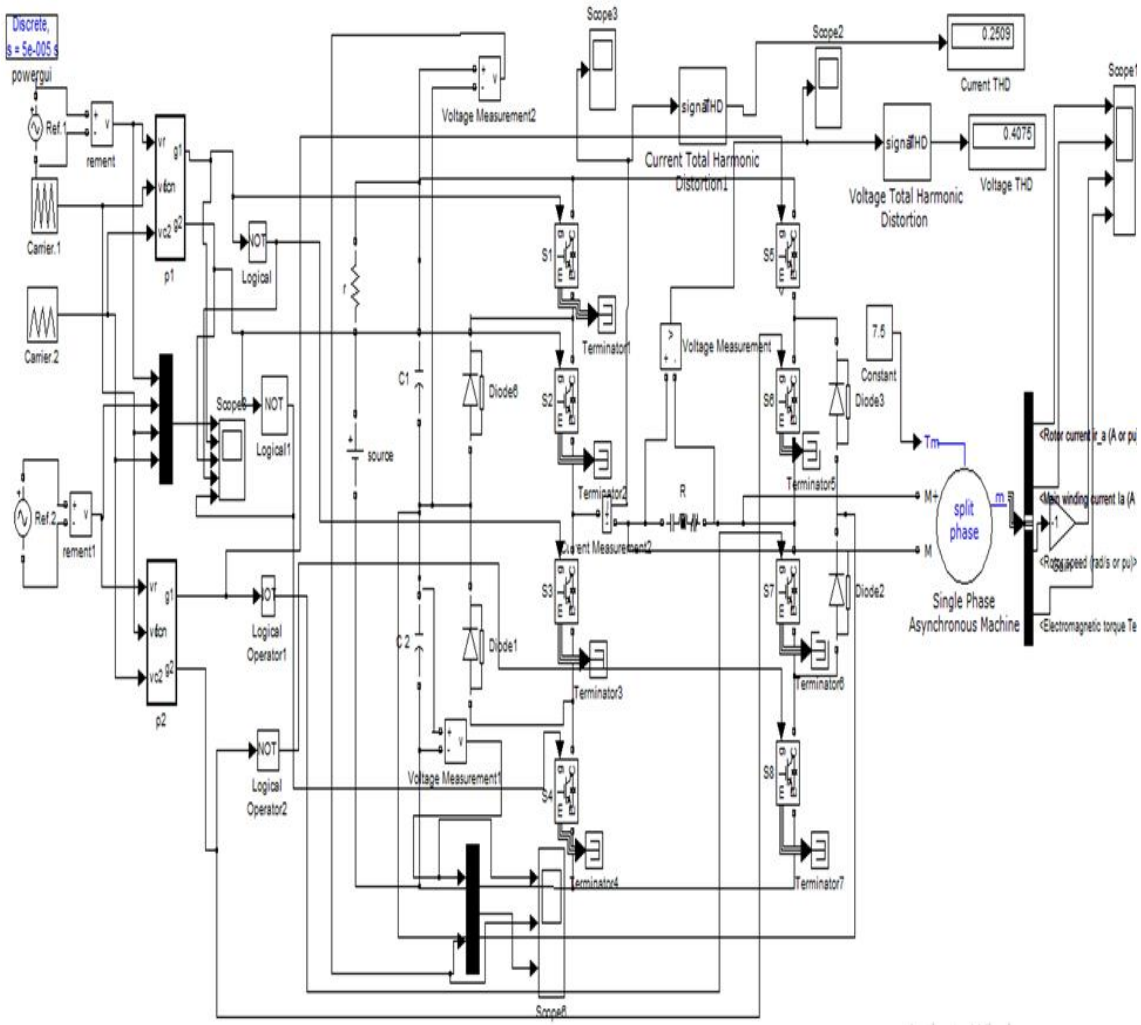

Figure 5: MATLAB/Simulink Model of Proposed circuit firing the power circuit

Figure 6 is the full range balanced input capacitor voltage of DC-biased enhanced unipolar modulation topology for DC -AC power converter-fed single-phase induction motor. It proves that Figure 6a and Figure 6b have equal 100V across C1 and C2 throughout the span of 5 seconds and even beyond without external circuitry added to Figure 5 unlike the convectional ones.

The output voltage of Figure 5 across motor load indicated stabilized five level line-to-line with peak voltage of 200V at $4.91 \leq t \leq 5$seconds that depicts pure sinusoidal wave in staircase form as shown in Figure 7

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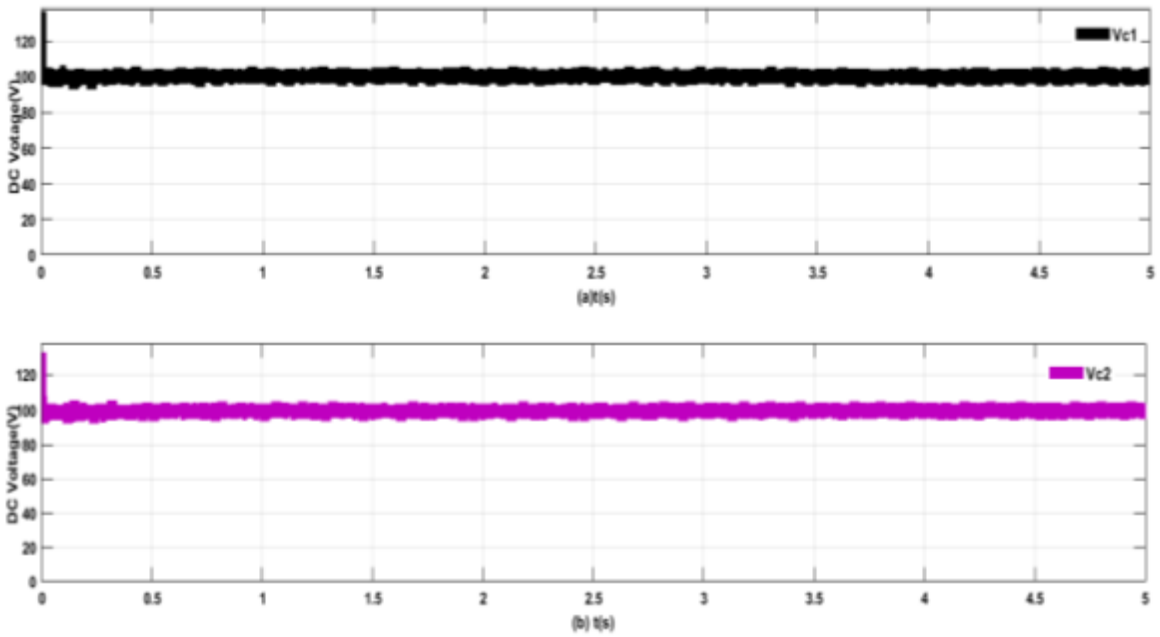

Figure 6: DC-biased enhanced unipolar modulation topology for DC -AC power converter-fed single-phase induction motor balanced capacitor

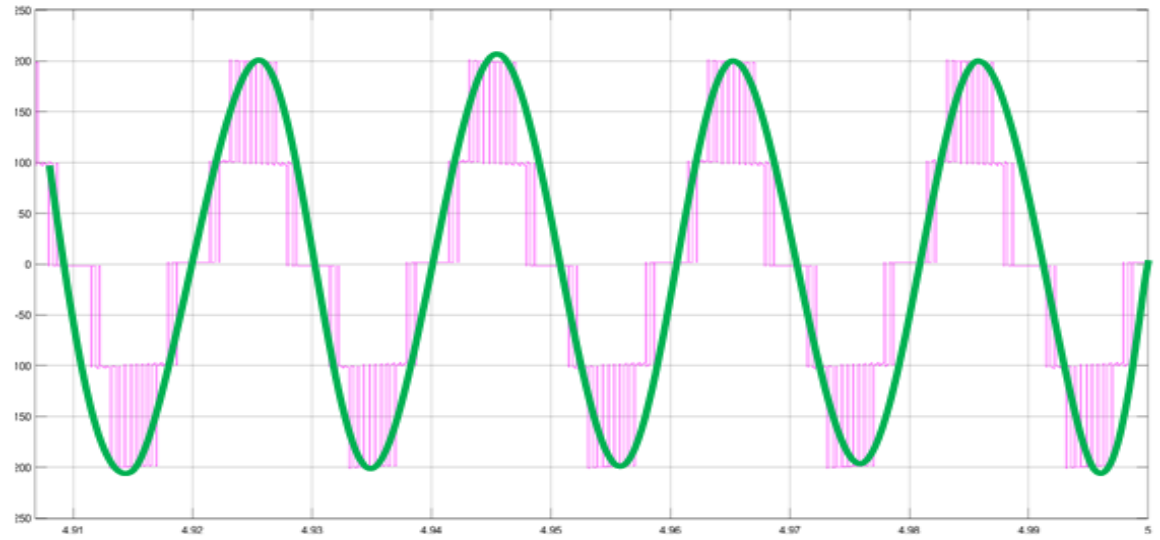

Figure 7: 5-level line-to-line output voltage waveform of the diode-clamped multilevel inverter

Figure 8 is the simulation of dynamic model of induction motor fed with inverter as modeled in equations (31) – (40) Comparing the results of the output motor speed of the inverter fed in Figures 9 and dynamic model in Figures 10 it is evident that the speed obtained from the dynamic model of the motor in Figure 10 which maintained its maximum at 900rpm was controlled, (V/f control) to a value of 200rpm in Figure 9 using research system to modulate Diode Clamp multilevel inverter. When the frequency (f) is decreased, by tuning the Duty ratio of research system the speed is reduced according to the relationship, $\text{speed}(n) = \frac{120f}{p}$

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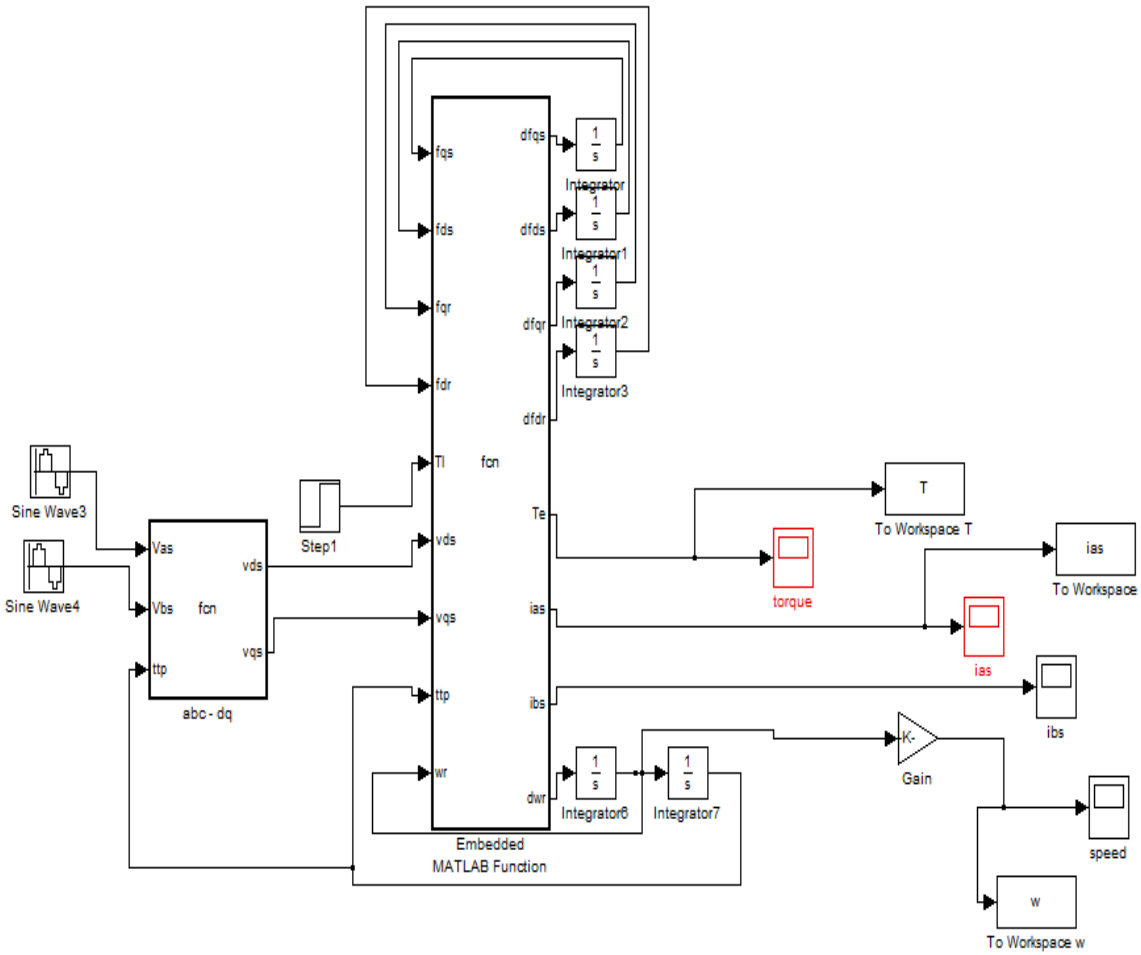

Figure 8: simulation of Single-phase induction motor dynamic model

It is also observed that corresponding to a controlled speed of Figure 9, the current in the d-q axis of Figure 11 is higher than that obtained from the dynamic model of Figure 12. This is because when the frequency is decreased; the voltage is increased thereby increasing the current as voltage is directly proportional to the current according to ohms law.

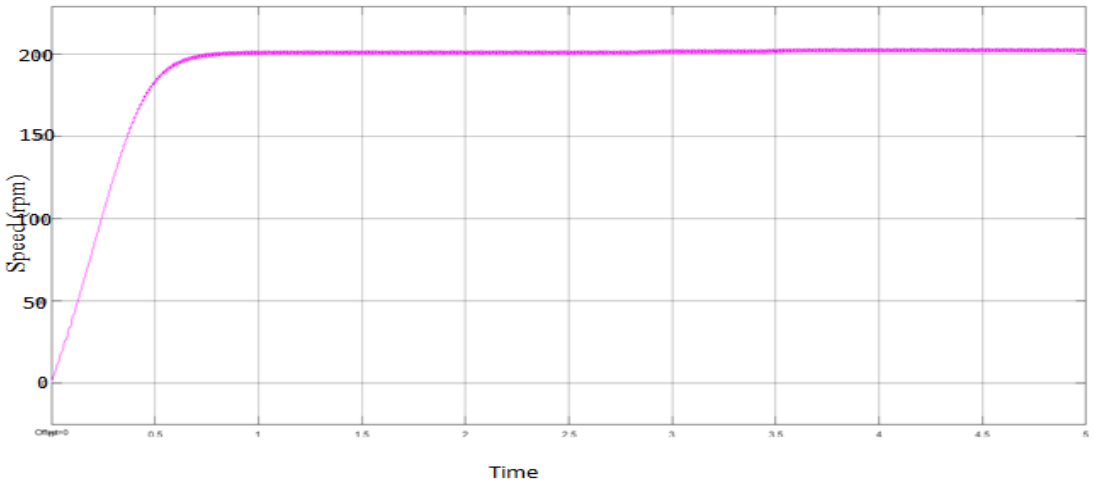

Figure 9: DC-AC power converter's fed-motor speed

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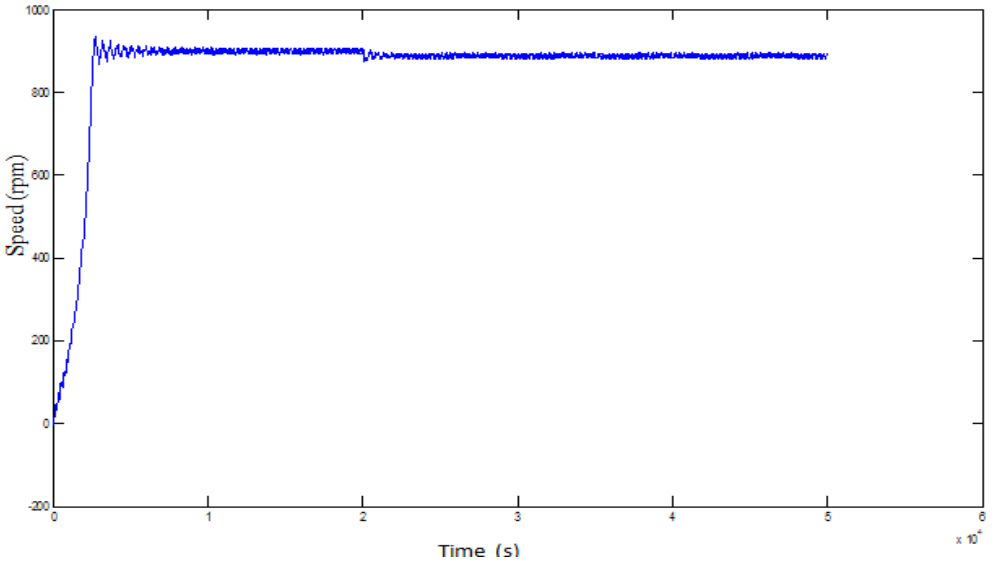

Figure 10: Dynamic model motor speed

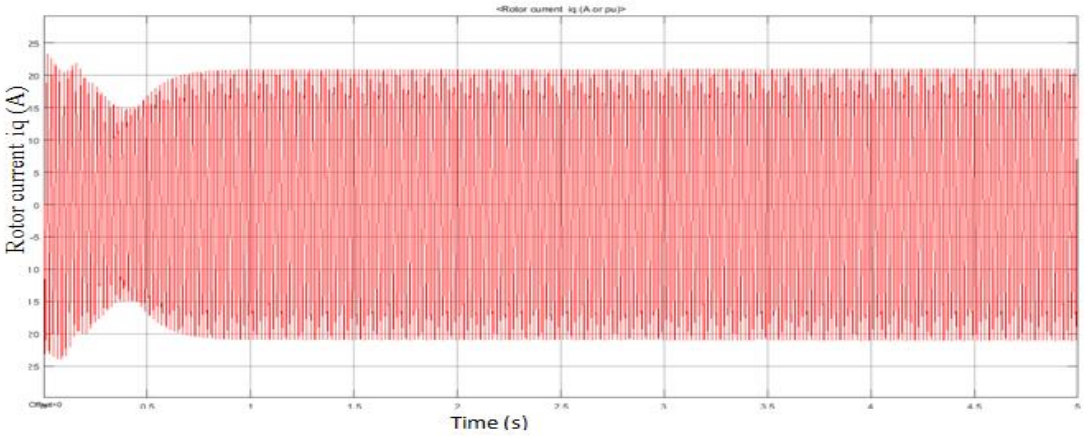

Figure 11: DC-AC power converter's fed rotor current in q-axis

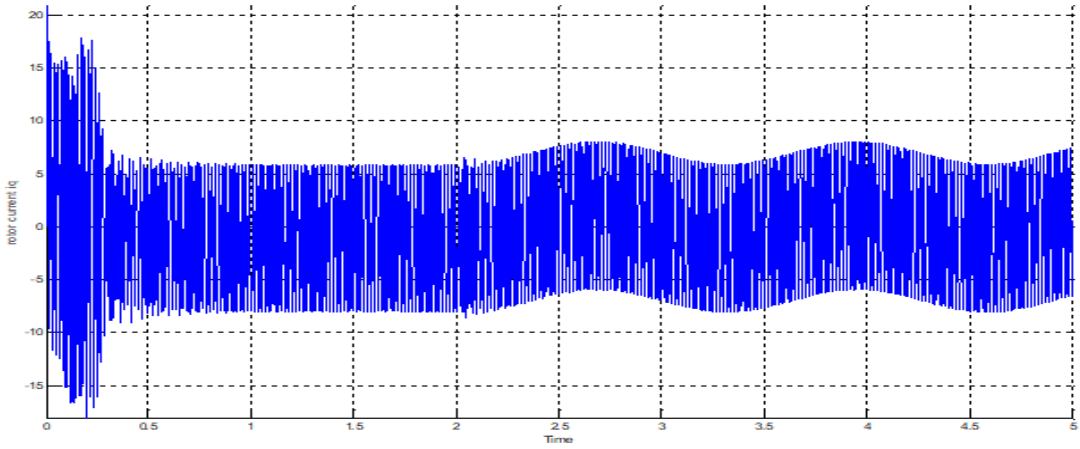

Figure 12: Dynamic model rotor current in q-axis

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7. EXPERIMENTAL RESULTS AND DISCUSSION

The digital oscilloscope display of the two modulating sine waves in Figure 13 has already been expressed in equations 26 and 27 likewise Figure 14 displayed implemented two zero-free carrier waves. Those carrier waves have been mathematically shown in equations 9 and 10. the positive zero-free carrier wave was compared with the modulating sine wave whereas zero-free negative carrier wave was compared with the 180^{o} phase shifted reference signal

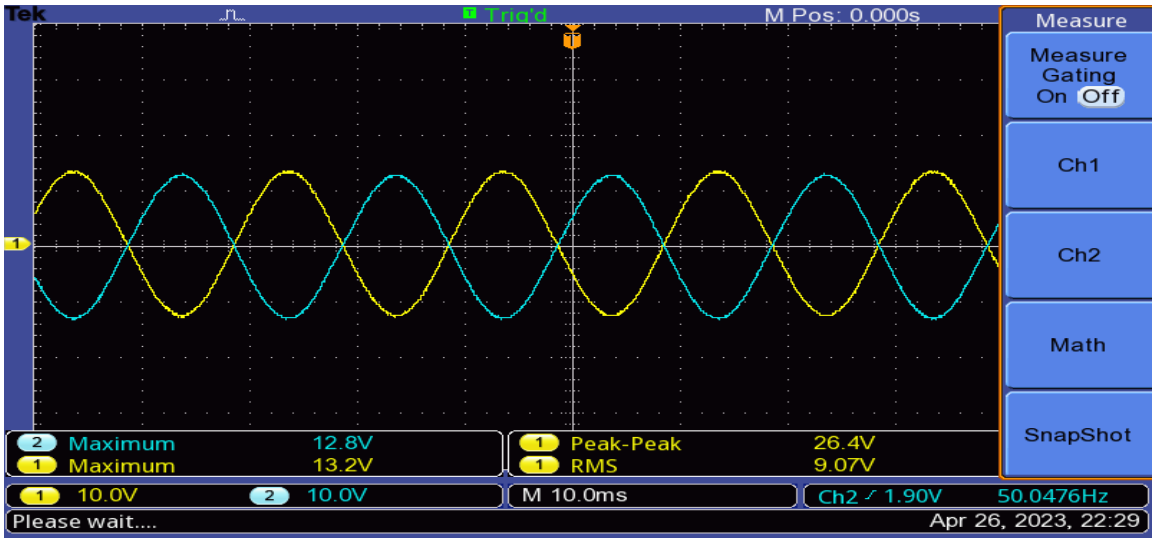

Figure 13: Experimented waveforms of two modulating reference voltages

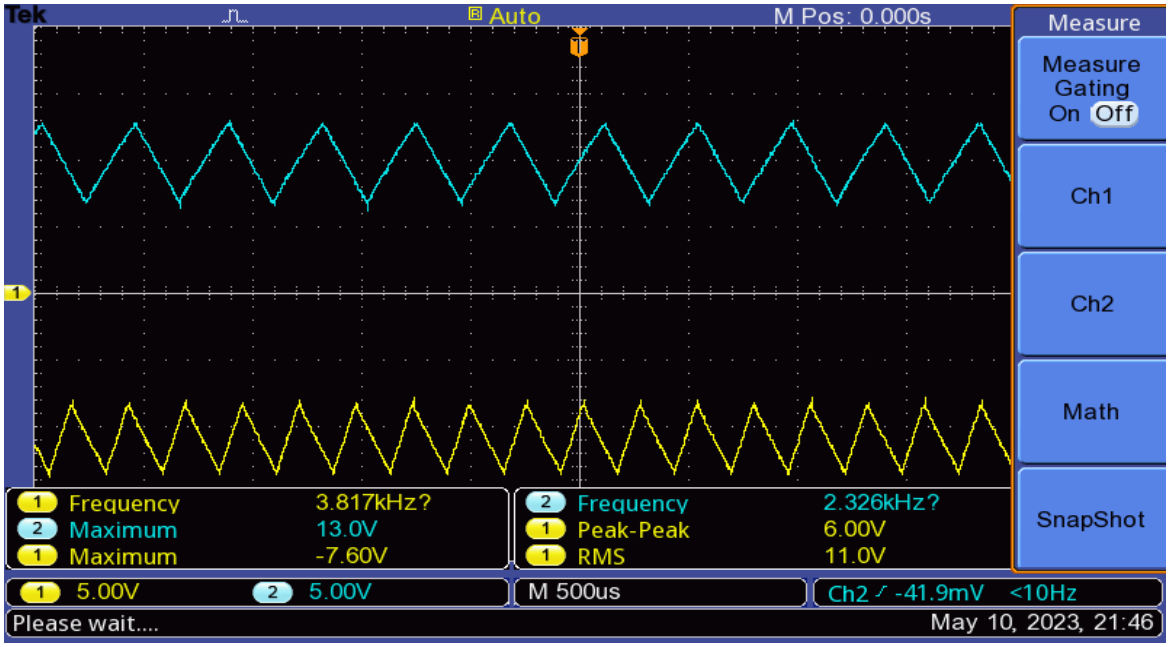

Figure 14: Experimented waveforms of carrier voltages

The triggering pulses were generated when the comparative results of the positive and the negative were further processed by Atmega328p and drivers (TLP 250 and VO3120). Figures 15 (a-d) showed generated triggering pulses for switching S1 to S8 as obtained from the output of the driver's circuit.

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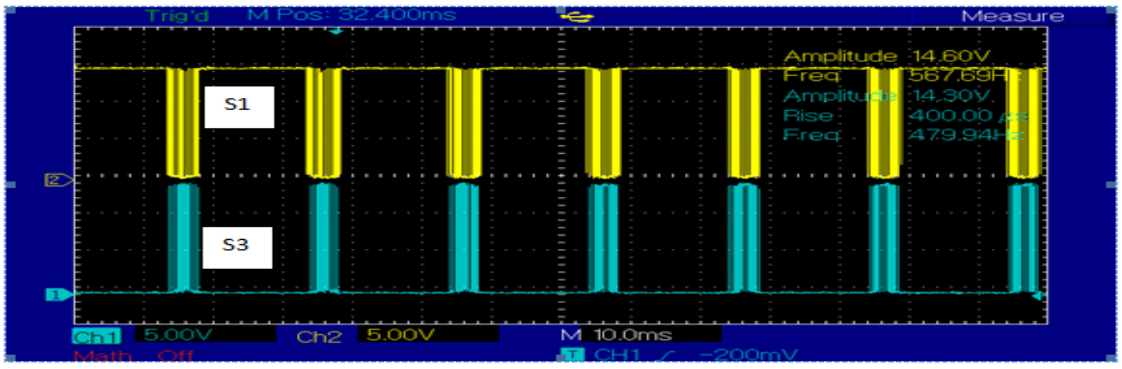
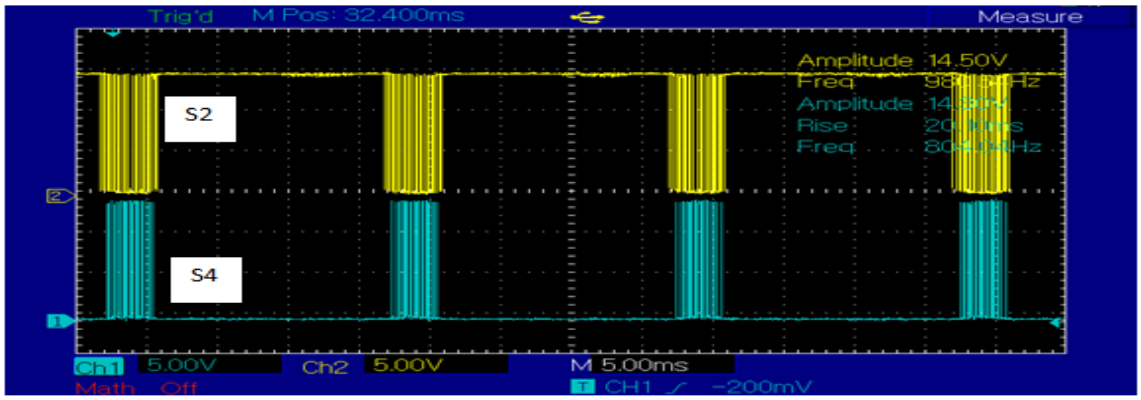


a



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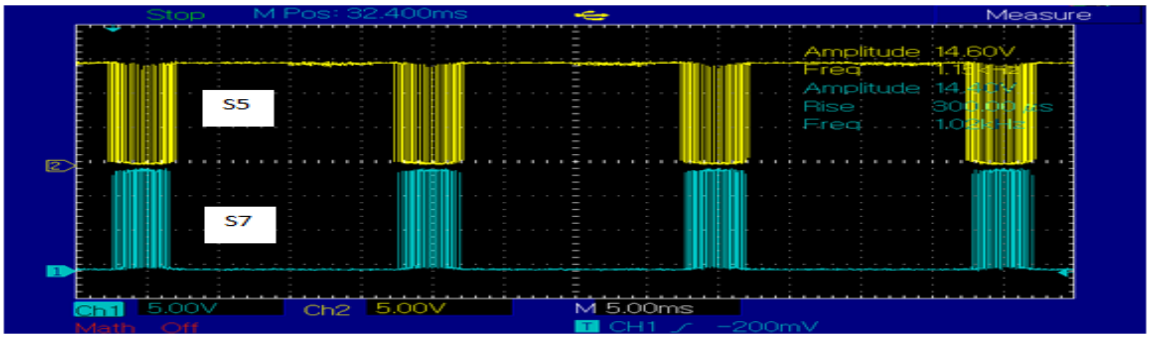
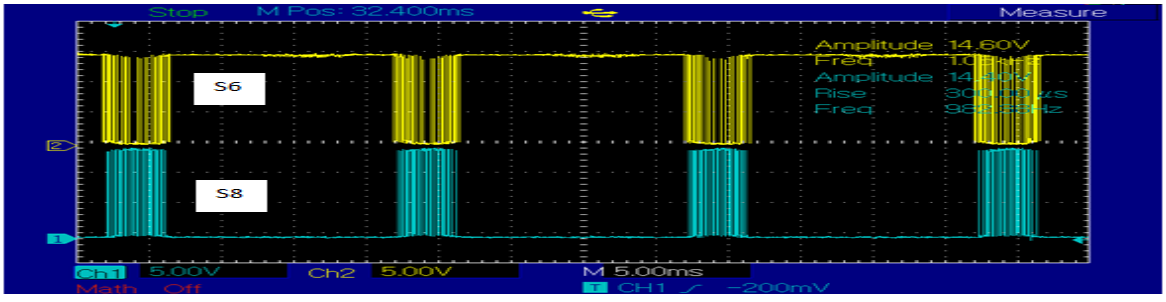


c



d

Figures 15 (a-d): Triggering pulses of research system

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It is worthy to note that, S1 complements S3, S2 complements S4, S5 complements S7 and S6 complements S8. Also Dead time is inserted at each of the complements using delay circuit to avoid shoot-through.

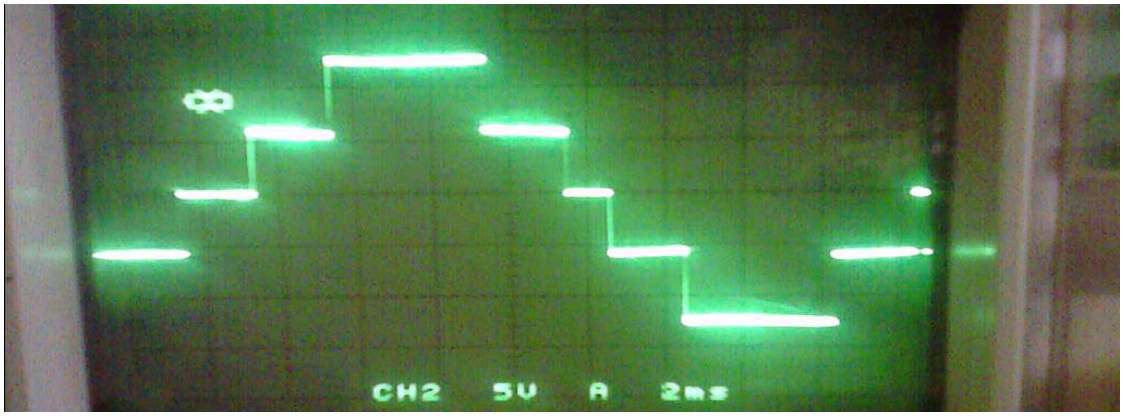
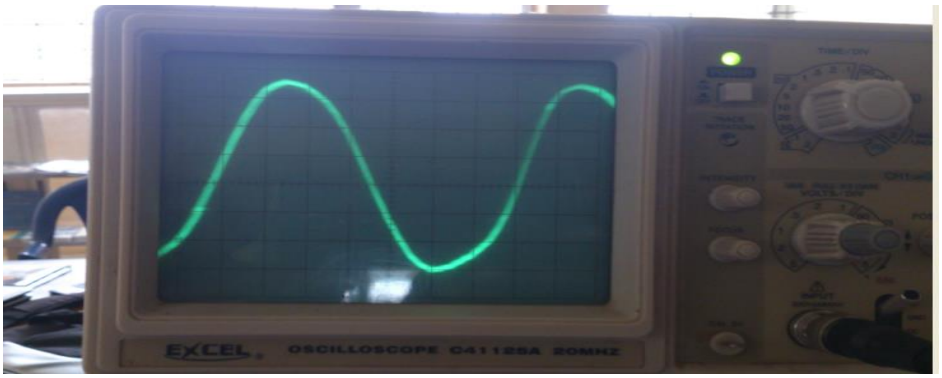
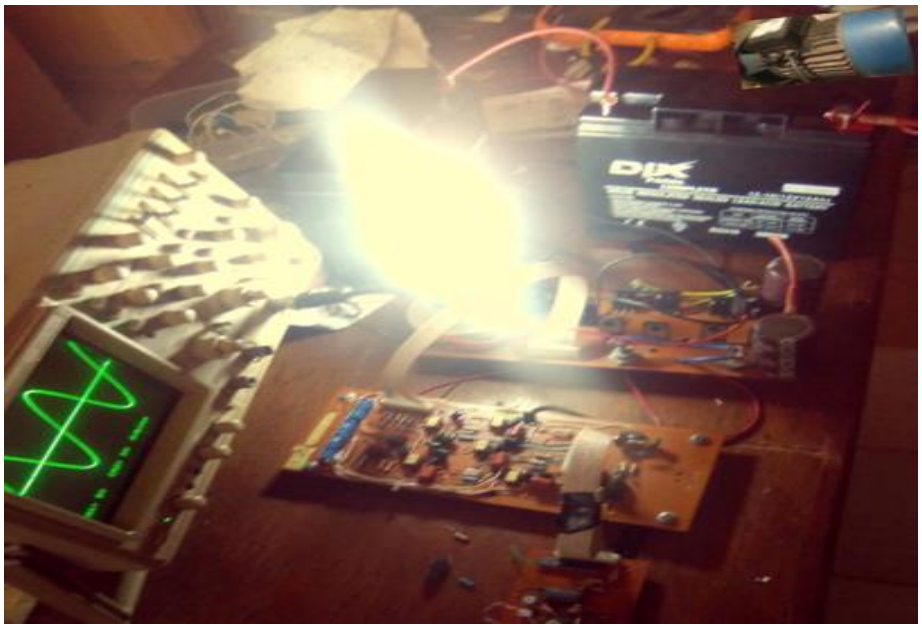


Figure 16: Experimented waveforms of 5-level line-to-line Output voltage of the MLI

Figure 16 displayed a stabilized five level line-to-line output voltage across an induction motor load devoid of drop at each level obtained using research system. The frequency and the corresponding amplitude modulation index used are Mf = 46.52 and Ma = 0.95





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8. CONCLUSION

Conventional Full Bridge five level diode-clamped multilevel inverter triggered with Dc-biased enhanced unipolar modulation topology that equally control single phase induction motor has been elucidated, modeled, simulated in MATLAB/Simulink software 2018/2021. The components values were sized and simulated in proteus 8 professional and was implemented in Laboratory of Innovative electronics using discrete electronic components, microcontroller and driver. Whereas the output waveforms of research system were captured on two channel digital oscilloscope, two channel analog oscilloscope was used to measure the output voltage waveform of multilevel inverter. The dynamic model of split phase single phase induction motor was simulated in embedded MATLAB 2009b to determine the running speed and compared with the speed of the same motor being controlled with research system powered inverter.

It was observed that constant speed induction motor was simply controlled (v/f) with research system which has less number of carrier signals, hence less bulky, easily packaged and cheaper in production far from conventional modulation schemes. The results produced by the proposed scheme on switching diode-clamped MLI are: voltage and current with total harmonic distortions of 0.4075% and 0.2509%, stabilized 200V output voltage and 20A output current, at frequency of 50Hz and output power of 4kw.

Recommendation for future research

The research system was developed and applied on conventional Diode clamp multilevel inverter to balance the active capacitor without considering the number of circuit component count of the inverter, therefore it is expedient that, it will in future research be applied in hybrid inverters with reduced component count. It is recommended that the stabilize voltage of 200V and current 20A obtained be upgraded to conventional grid utility voltage of 220/240V by increasing the source voltage to accommodate loses.

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